DAEWOO

Service Manual

59 / 66 Cm **STEREO Colour Television**

CHASSIS : CP-775

MODEL : 2594ST / 2896ST
2898ST

DAEWOO ELECTRONICS CO., LTD.

CONTENTS

■ Specifications

CRT	25" : A59EAK071X11 (PHILIPS) 28" : A66EAK071X11 (PHILIPS)
System	TF : PAL - B/G for West Europe, NTSC-3.58 / 4.43 (Play back) TA : PAL - B/G, SECAM-L/L' for France, NTSC-3.58 / 4.43 (Play back) TU : PAL- I for U.K, NTSC-3.58 / 4.43 (Play back) TK : PAL/SECAM - B/G, D/K, NTSC-3.58/4.43(play back) for East Europe & CIS
Main Voltage	230V AC, 50Hz
Power Consumption	Stand-by mode : 10 Watts Normal operating mode : 25" = 75 Watts 28" = 75 Watts
Sound output	5 + 5 Watts, 10 % THD at RF 60 % mod. (1 ㎑)
Speaker	12W 4 ohm x 2 EA
Antenna Impedance	75 ohm unbalanced input
Tuning system	VS(voltage synthesis) tuning
Tuner	3303KHC (TF, TA, TK, TI Model) BAND I : CH2 - CH4 BAND III : CH5 - CH12 CABLE BAND : S1' - S3' , S1 - S20 HYPER BAND : S21 - S41 BAND IV, V : CH21 - CH69 DT2-IV17D (TU Model) BAND IV, V : CH21 - CH69
Number of program	70 programs
Aux. Terminal	21 pin EURO-SCART jack (AV input, TV output, RGB input) 21 pin EURO-SCART jack (AV input, S-VHS input) RCA type AV input jack Headphone jack (3.5 mm ϕ)
Remote controller	R-28B03 or R-35D05 with 2 "AA" type batteries
Teletext	8 pages memory TOP & FLOF - West option :English, German/Dutch/Flemish, French, Italian, Spanish/Portuguese, Swedish/Finnish/Danish, Czech/Slovak - East option : Polish, Czech/Slovak, Rumanian, Hungarian, Servo-croat, German/Dutch/Flemish, French, Italian - Turkish option : Turkish, English, German/Dutch/Flemish, French, Italian, Spanish/Portuguese, Swedish/Finnish/Danish - Cyrillic option: Russian, Lettish/Lithuanian, Estonian, Ukranian, Czech/Slovak, Servo-croat, English
OSD language	-East,West,Turkish Version : English,French,German,Italian,Spanish -Cyrillic Version : Russian, English, German

■ Alignment Instructions

1. AFT

1.1 Standard B/G,D/K,I and L

1) Set a Signal Generator with
   - RF FREQUENCY = 38.9 MHz,
   - RF OUTPUT LEVEL = 80 ±5 dBuV
   - System = PAL / SECAM - B/G, D/K, I
2) Connect the Signal Generator RF Output to P101 (Tuner IF Output).
   There must be no signal input to the tuner.
3) Press the "AFT" KEY and wait until the TV screen display "AFT OK".

1.2 Standard SECAM-L' (France VHF-Low)

* Above mentioned "1.1" adjustment has to be done in advance.

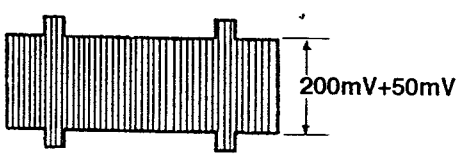
1) Set a Signal Generator with
   - RF FREQUENCY = 34.5 MHz,
   - RF OUTPUT LEVEL = 80 ±5 dBuV
   - System = SECAM - L'
2) Connect the Signal Generator RF Output to P101 (Tuner IF Output).
   There must be no signal input to the tuner.
3) Press the "L' AFT" KEY and wait until the TV screen display "L AFT OK".

2. AGC

1) Set a Pattern Generator with RF LEVEL 63 ±2 dBuV .
2) Connect a OSCILLOSCOPE PROBE to P101 (TUNER AGC INPUT).
3) Adjust AGC UP/DOWN KEY the voltage drop 1V dc over below its maximum voltage.

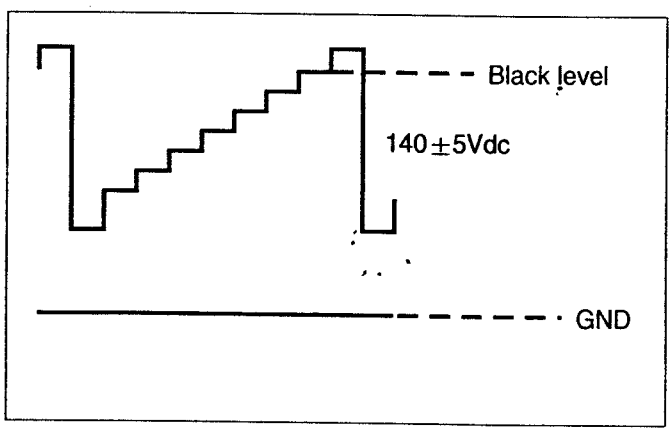
* Alternative Method

1) Set a Pattern Generator with
   - RF LEVEL 80 ±5 dBuV
   - PAL CROSSHATCH
   (without SOUND CARRIER)
2) Connect a OSCILLOSCOPE
   (Bandwidth ≥ 100MHz) PROBE
   to P101 (TUNER IF OUTPUT).
3) Use AGC UP/DOWN KEY to obtain
   an envelop amplitude 200 + 50 mVp-p.



3. SCREEN

1) Apply a COLOR BAR pattern signal.
2) Set the CONTRAST, BRIGHTNESS
   to MAX, COLOR to MIN.
3) Set the R,G,B LEVEL to CENTER (31/63)
   with R,G,B UP/DOWN KEY.
4) Connect a OSCILLOSCOPE PROBE
   to P906 (CRT CATHOD R, G, B).
5) Adjust the SCREEN VOLUME on FBT
   such that the highest black level voltage
   140 ±5Vdc.



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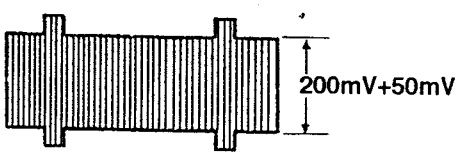

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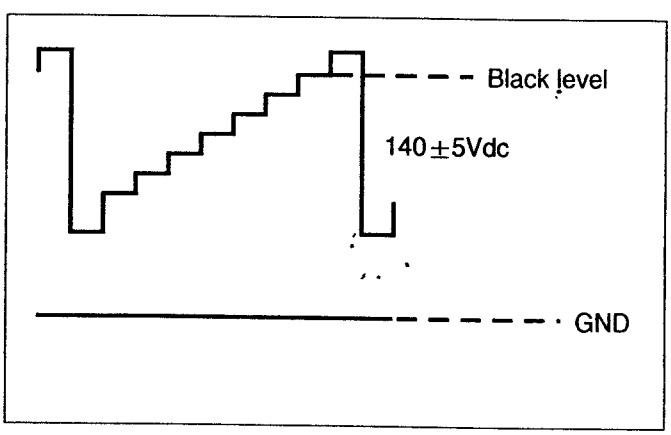


4. WHITE BALANCE

1) Set the TV to NOR I mode.
2) Set the R,G,B LEVEL to CENTER with R,G,B UP/DOWN KEY .
3) Adjust the R,G,B UP/DOWN KEY of the other color which did not appear on the screen to obtain WHITE.

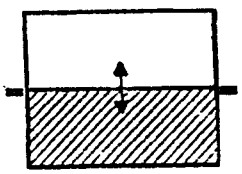
5. FOCUS

1) Apply a RETMA PATTERN signal.
2) Adjust the FOCUS VOLUME on FBT to obtain optimal resolution.

6. GEOMETRY

6.1 VERTICAL CENTER

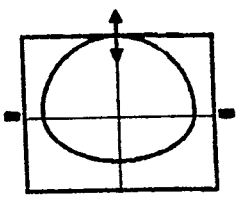
1) Set the TV to NOR I mode.
2) Pressing the V-SIZE UP/DOWN KEY, the lower half of the screen is blanked.
3) Adjust the border line of blanked picture coincident with the mechanical center marks of the CRT using the V-SIZE UP/DOWN KEY.



6.2 VERTICAL SIZE

* The VERTICAL CENTER adjustment has to be done in advance.

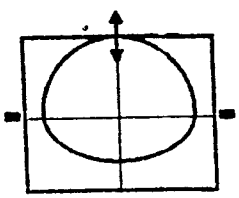
1) Apply a RETMA PATTERN signal.
2) Set the TV to NOR I mode.
3) Adjust the upper part of the picture with the V-SIZE UP/DOWN keys.



6.3 VERTICAL SLOPE

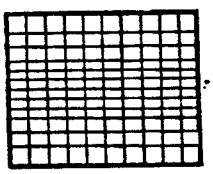
* The VERTICAL SIZE adjustment has to be done in advance.

1) Apply a RETMA PATTERN signal.
2) Adjust the lower part of the picture with the V-SLOPE UP/DOWN keys.



6.4 VERTICAL S-CORRECTION

1) Apply a CROSSHATCH PATTERN signal.
2) Adjust the S-COR UP/DOWN KEY to obtain the same distance between horizontal lines.



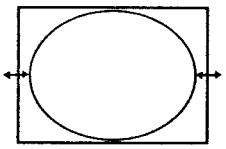
6.5 HORIZONTAL CENTER

1) Apply a RETMA PATTERN signal.
2) Adjust picture centering with CENTER LEFT/RIGHT keys.

7. EW

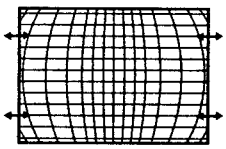
7.1 WIDTH

1) Apply a RETMA PATTERN signal.
2) Pressing the EW KEY, the WIDTH OSD appear in the screen.
3) Adjust the over to make a perfect circle with VOL-UP/DOWN KEY.



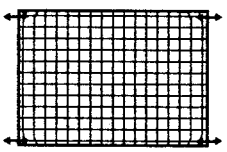
7.2 PARA

1) Apply a CROSSHATCH PATTERN signal.
2) Pressing the EW KEY, the PARA OSD appear in the screen.
3) Adjust the vertical line to straight with VOL-UP/DOWN KEY.



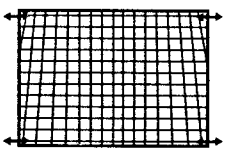
7.3 CORNER

1) Apply a CROSSHATCH PATTERN signal.
2) Pressing the EW KEY, the CORNER OSD appear in the screen.
3) Adjust the vertical line to straight with VOL-UP/DOWN KEY.



7.4 TRAPI

1) Apply a CROSSHATCH PATTERN signal.
2) Pressing the EW KEY, the TRAPI OSD appear in the screen.
3) Adjust the vertical line to straight with VOL-UP/DOWN KEY.

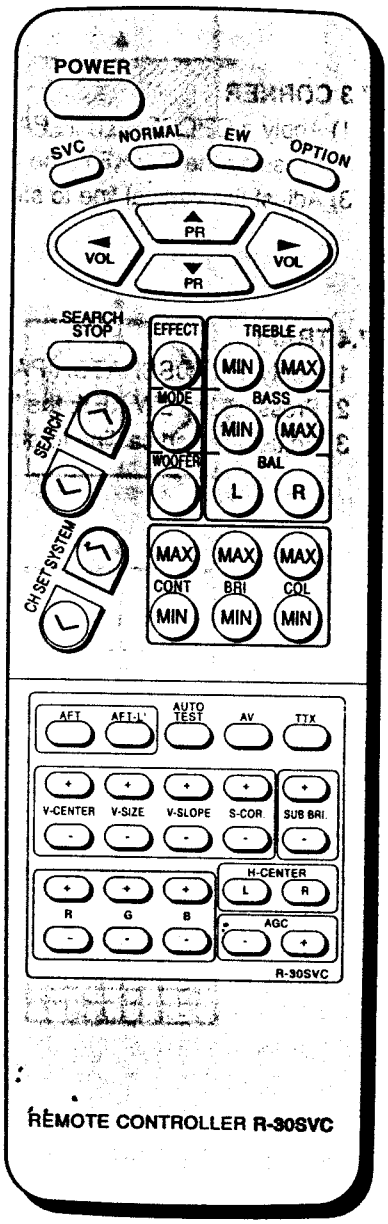


If EEPROM (I702) has been changed ;
- Option data has to be changed and
- all alignment function has to be readjusted .

*The initial state of adjustment are as follows;

	28TAF	28TUF	28TFF
TUNER	3303KHC	DT21V17D	3303KHC
LANGAGE	French	English	English
W/B	RGB = 32	32	32
AGC	11	9	10
V-CENTER	30	37	30
V-SIZE	52	54	52
V-SLOPE	27	28	27
S-COR	15	15	15
H-CENTER	43	42	42
WIDTH	63	63	62
PARA	36	38	37
CORNER	30	28	30
TRAPI	29	28	29

*Service Remocon



■ SIF ADJUSTMENT

1. APPARATUS CONNECTION & PRESETTING

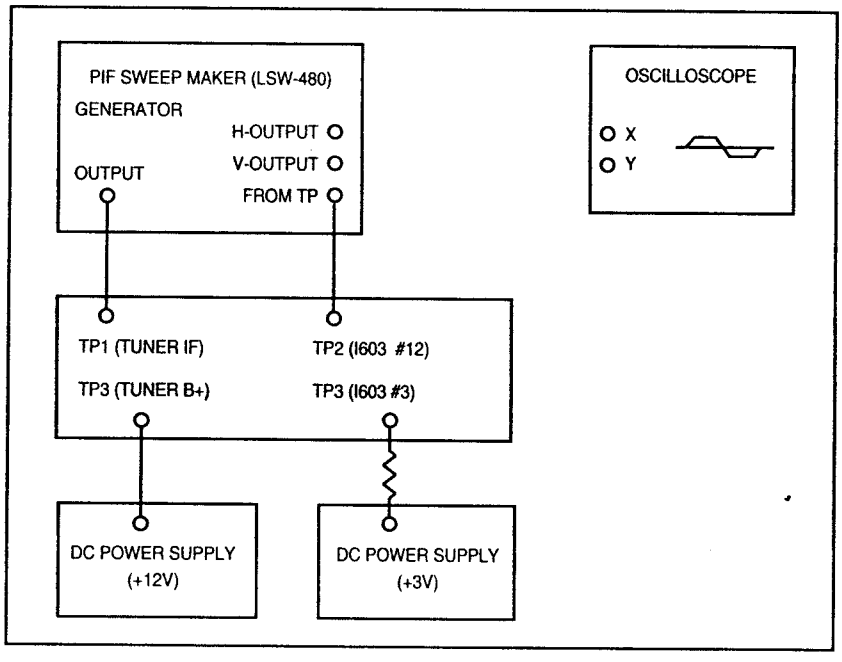
* CONNECTION

1) Connect H-out of LSW-480 to X-axis of the oscilloscope and V-out of LSW-480 to Y-axis of the oscilloscope.
2) Connect the sweep signal output to TP1.
3) Set ATTENUATOR of LSW-480 to 20dB.
4) Supply 12V D.C. voltage(B+) to TP3.
5) Supply 3V D.C. voltage(B+) to TP4.
6) Connect the test point of LSW-480 to TP2.
7) Adjust L109(AFT COIL) so that the P marker point is located on the reference level.

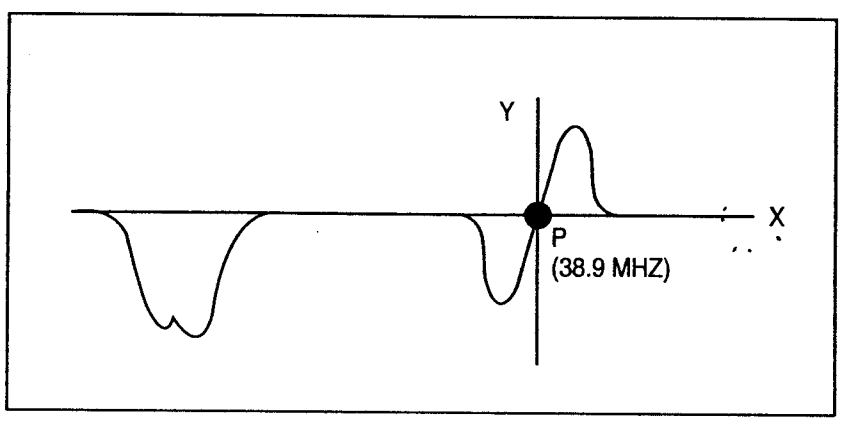
* PRESET

1) Oscilloscope Scaling
   a) Put the scale of X and Y of the oscilloscope to D.C. level
   b) Set the horizontal time display to X-Y.
   c) Put the horizontal axis (x) to 1V / div. and the vertical axis (Y) to 2V / div.
2) LSW-480 MARKER FREQ. SETTING

fp(n+1)	fs	fc	fp-2	fp	fs(n-1)
31.9	33.4	34.47	36.9	38.9	40.4



- Connection For SIF Adjustment -



■ IC Description

DW5255S*(Micro-controller & West/East Teletext Decoder)

(1) General Description

The TDA5255 contains a slicer for VPS and TTX, an accelerating acquisition hardware module, a display generator for "LEVEL 1" TTX data and a 8 bit u-controller running at 333 nsec cycle time.
The controller with dedicated hardware guarantees flexibility, does most of the internal processing of TTX acquisition , transfers data to/from the external memory interface and receives/transmits data via I2C and UART user interfaces.
The Slicer combined with dedicated hardware stores TTX data in a VBI 1Kbyte buffer.
The u-controller firmware does the total acquisition task (hamming- and parity -checks, page search and evaluation of header control bits) once per field.

(2) Feature

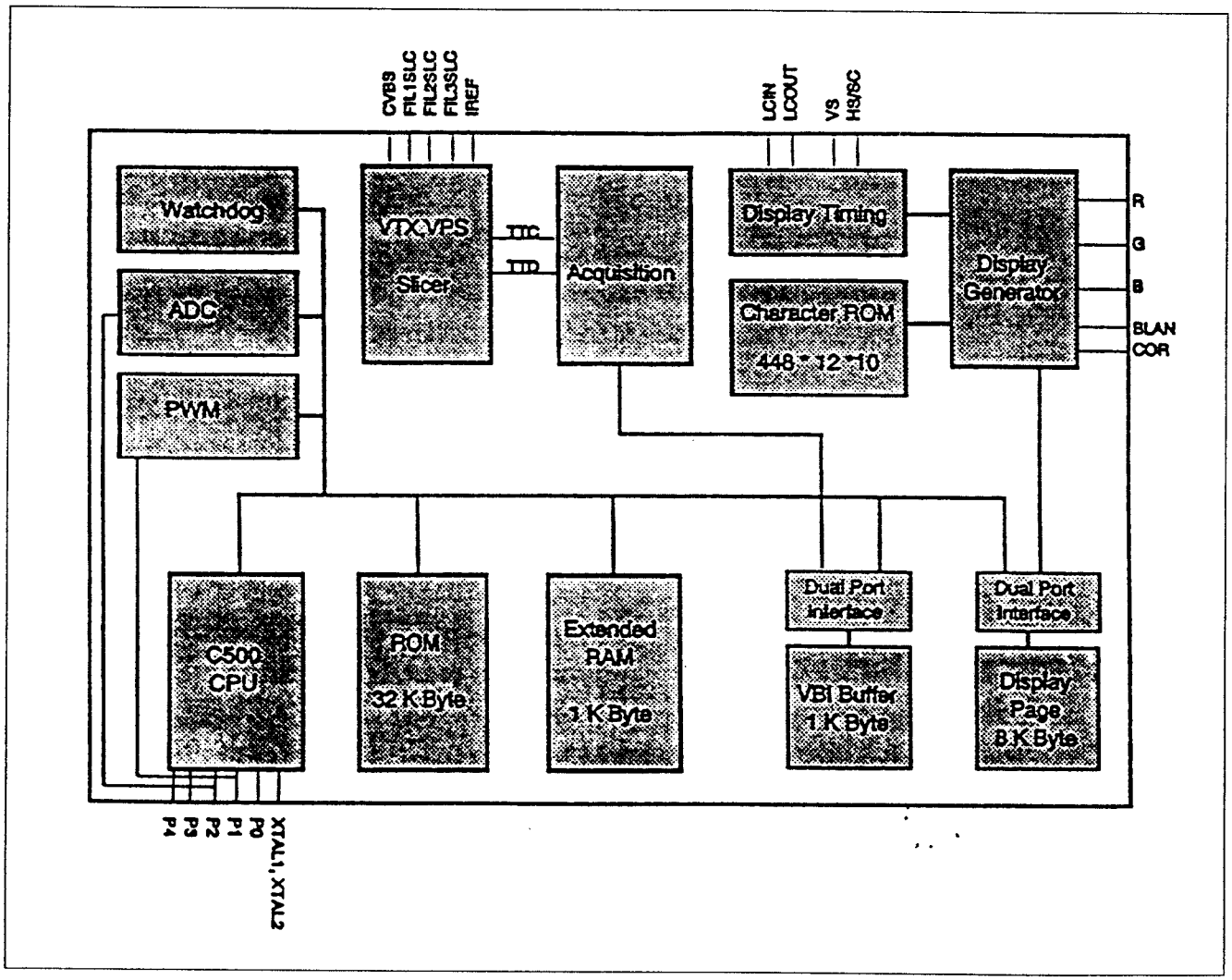
- **Acquisition**:
  - feature selection via special function register
  - simultaneous reception of TTX and VPS
  - fixed framing code for VPS and TTX
  - programmable framing code window for TTX
  - Acquisition during VBI
  - direct access to VBI RAM buffer
  - Acquisition of packets x/26, x/27, 8/30 (firmware)
  - assistance of all relevant checks (firmware)
  - 1-bit framing-code error tolerance (switchable)
- **. Display:**
  - features selectable via special function register
  - 50/60 Hz display
  - level 1 serial attribute display pages
  - blanking and contrast reduction output
  - 8 direct addressable display pages
  - 12 x 10 character matrix
  - 96 character ROM (standard G0 character set)
  - 143 national option characters for 11 languages
  - 288 characters for X/26 display
  - 64 block mosaic graphic characters
  - 32 free addressable characters for OSD in expanded character ROM + 32 inside OSD box
  - double height (TOP/BOTTOM)
  - conceal/reveal
  - transparent foreground/background -inside/outside of a box
  - cursor (colour changes from foreground to background colour)
  - flash (flash rate 1s)
  - programmable horizontal und vertical sync delay
  - hardware assisted fast display page erase
  - full screen background colour in outer screen
- **Synchronization**:
  display synchronization to sandcastle or Horizontal Sync (HS) and Vertical Sync (VS) with startstop-oscillator or
  display synchronization to sandcastle or Horizontal Sync and Vertical Sync with external clock
  independent clock systems for acquisition, display and controller
- **Controller:**
  - 8 bit configuration
  - 18 MHz internal clock
  - 0.33 us instruction cycle
  - eight 16-bit data pointer registers (DPTR)

- two 16-bit timers
- watchdog timer
- serial interface (UART)
- 256 bytes on-chip RAM
- 1 Kbyte on-chip extended RAM (access via MOVX)
- 8 Kbyte on-chip ACQ-buffer-RAM (access via MOVX)
- 6 channel 8-bit pulse width modulation unit
- 2 channel 14-bit pulse width modulation unit
- 4 multiplexed ADC inputs with 8-bit resolution
- one 8-bit I/O port with open drain output and optional I2C emulation
- two 8-bit multifunctional I/O ports
- one 4-bit port working as digital or analog inputs
- one 2-bit I/O port with optional address latch enable function

• **P-SDIP 52 package**

• **5 V supply voltage**

(3) Block Diagram



Pin	Name	Symbol	Description
1	P3.1	SYS	SECAM-L' OUT for switching SAW filter L9461 - SECAM-L' : H - SECAM- L : L
2	P0.7/Open Drain	BUSSTOP	I2C BUS STOP IN for Computer controlled alignment in Factory (Active Low)
3	P0.6/Open Drain	SDA	Serial data IN/OUT for I2C
4	P0.5/Open Drain	SCL	Serial clock IN/OUT for I2C
5	P0.4/Open Drain	OPTION	#5 #6 Teletext
6	P0.3/Open Drain	OPTION	H H West Teletext L H East Teletext H L Turkish Teletext
7	P0.2/Open Drain	OPTION	#7 #8 #17 Tuning / Sound System
8	P0.1/Open Drain	OPTION	L H H B/G (2-G, NICAM) H H H B/G, D/K (2-C, NICAM) L L H I/I (NICAM) H L H I (UHF only, NICAM) H H L L/L' →B/G (2-C, NICAM) L H L B/G →L/L' (2-C, NICAM)
9	P0.0/Open Drain	LED	LED drive OUT - Stand-by mode : H - Operating mode : L (IR reception : pulse)
10	VSS	VSS	ground
11	VCC	VCC	Power Supply
12	XTAL1	OSCIN	Input to inverting osc. Amplifier
13	XTAL2	OSCOUT	Output of inverting osc. Amplifier
14	P4.0/ALE		Not Used
15	RESET	RST	RESET IN (ACTIVE LOW)
16	P1.7/14BIT PWM	VT	TUNING VOLTAGE OUT
17	P1.6/14BIT PWM	OPTION	TUNING SYSTEM
18	P1.5/14BIT PWM	F/SW	F/SW IDENT IN for stopping OSD display in RGB mode - H : TV /AV mode - L : RGB mode
19	P1.4/14BIT PWM	OPTION	ATS OPTION H : ON L : OFF
20	P1.3/14BIT PWM	MUTE	AUDIO MUTE OUT
21	P1.2/14BIT PWM	GND	GND
22	P1.1/8BIT PWM		Not Used
23	P1.0/8BIT PWM		Not Used

Pin	Name	Symbol	Description
24	VSSA	VSSA	Analog GND for Slicer
25	FIL3	FIL3	PLL Loop Filter I/O for Phase Shifting
26	FIL2	FIL2	PLL Loop Filter I/O for TTX Slicing
27	FIL1	FIL1	PLL Loop Filter I/O for VPS Slicing
28	VCCA	VCCA	Analog Supply for Slicer
29	IREF	IREF	Reference Current for Slicer PLLs
30	CVBS	CVBS	CVBS IN
31	P2.3/8 bit ADC		Not Used
32	P2.2/8 bit ADC	AGC	IF AGC INPUT for Auto Tuning System
33	P2.1/8 bit ADC	KS	Local KEY SCAN IN
34	P2.0/8 bit ADC	S/SW	S/SW IDENT IN for Automatic switching between TV/AV mode - H : AV / RGB mode - L : TV mode
35	VSS VSS-OSD	VSS	Ground
36	P3.3/INT1	IR	REMOTE IR IN
37	VDD VCC-OSD	VDD	Power Supply
38	LCIN OSCIN-OSD	LCIN	CLOCK IN for OSD
39	LCOUT	LCOUT	CLOCK OUT for OSD
40	P3.7/TXT I/O	BL	BAND VHF-L OUT (Active High)
41	P3.6/RXD	BH	BAND VHF-H OUT (Active High)
42	P3.5/T1	BU	BAND UHF OUT (Active High)
43	P3.4/T0	POWER	POWER CONTROL OUT
44	P3.2/INT0		Not Used
45	HS/SC	HSYNC	HOR. SYNC. IN (Active High)
46	P4.7/VS	VSYNC	VERT. SYNC. IN (Active High)
47	R	R	RED OUT
48	G	G	GREEN OUT
49	B	B	BLUE OUT
50	BLANK	BL	BLANK OUT
51	COR	COR	Not Used (CONTRAST REDUCTION OUT)
52	P3.0 T1C2/PWM1	EVEN/ODD	EVEN/ODD OUT for non-interlacing in TTX mode

CAT24C08P (E² PROM)

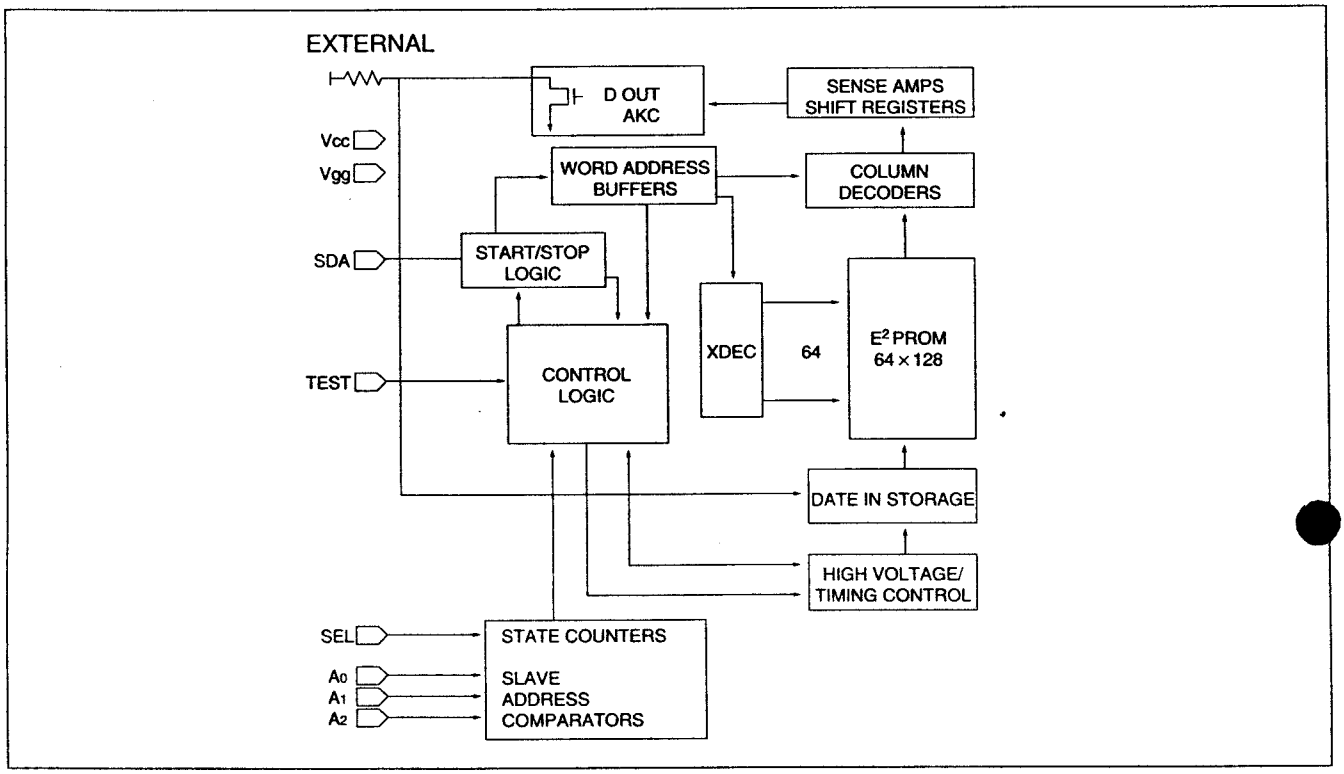
(1) Typical Features

- IC Bus compatible
- Low power CMOS Technology
- 16 Byte page write Buffer
- Self-Timed Write cycle with Auto-Clear
- 100,000 program/Erase cycles
- 100 Year Data Retention
- Optional High Endurance Device Available

(2) Description

The CAT24C08P is a 8K bit serial CMOS E^2 PROM internally organized as 1024x8bits. The CAT 24C08P features a 16 byte page write buffer.

(3) Block Diagram



(4) Pin Description

PIN	SYMBOL	DESCRIPTION
1-3	A0, A1, A2	Device Address Inputs
4	Vss	Ground
5	SDA	Serial Data/Address
6	SCL	Serial Clock
7	TEST	Connect to Vss
8	Vcc	+5V Power supply

TDA8375A (Single chip TV Processor for Negative modulation IF)

(1) General Description

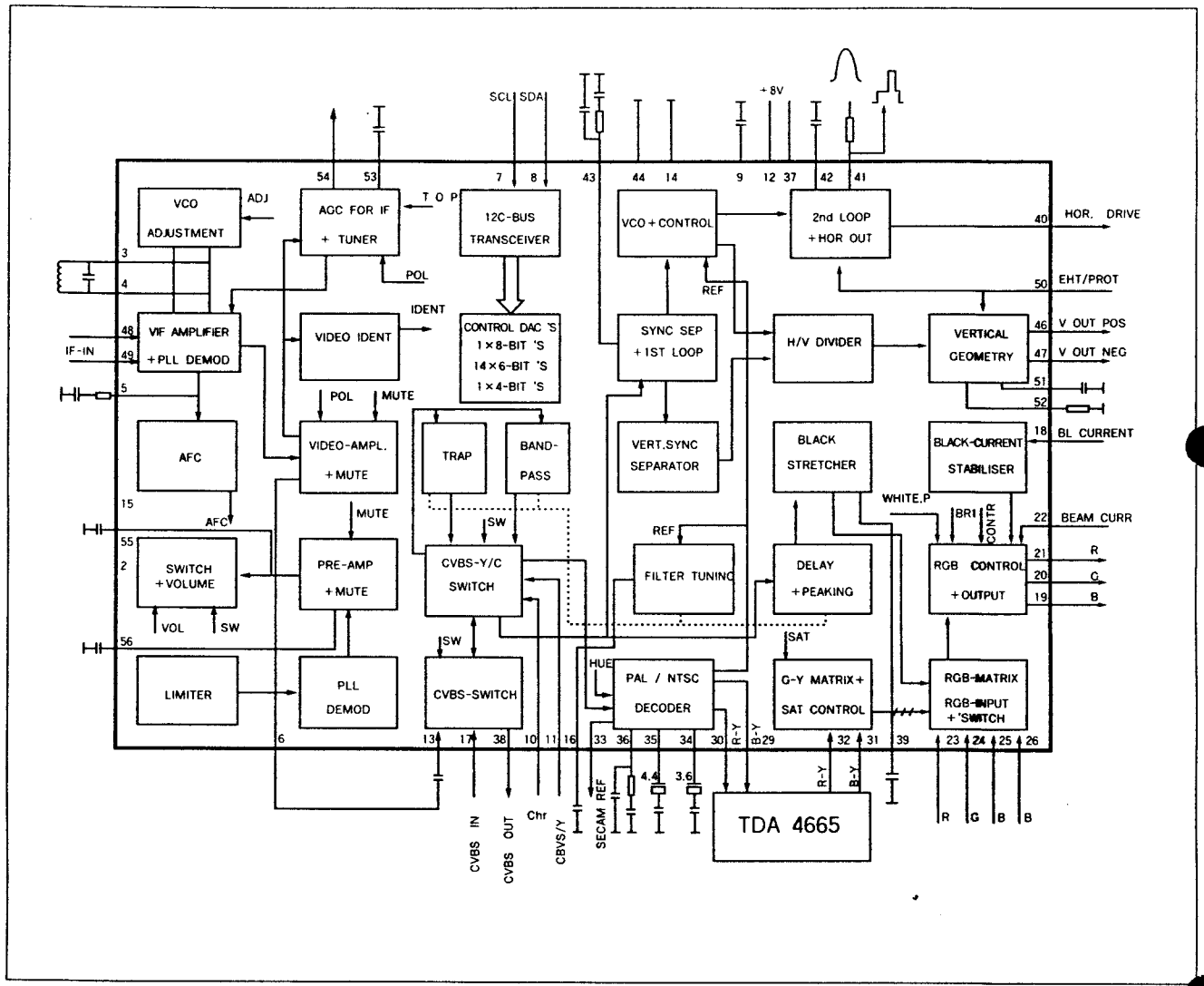
The TDA8375A is I2C-bus controlled single chip TV processors which are intended to be applied in PAL/NTSC television receiver.

The IC is mounted in a S-DIL 56 envelope.

(2) Feature

- **IF**
  - Vision IF amplifier with high sensitivity and good figures for differential phase and gain
  - PLL demodulator with high linearity offering the possibility for (single standard) intercarrier stereo audio application .
  - Alignment PLL via I2C
  - [TDA8375A] Multistandard IF with negative and positive modulation, switchable via I2C
- **Video**
  - Integrated luminance delay line
  - Integrated chroma trap and bandpass filters (auto calibrated)
  - Asymmetrical peaking circuit in the luminance channel
  - Black stretching of non standard CVBS or luminance signals
- **Colour**
  - SECAM interface for application with SECAM add-on TDA8395.
- **RGB**
  - RGB control (brightness, contrast, saturation)
  - Black current stabilization and white point adjustment
- **Input / Output**
  - Flexible video source select with CVBS input for the internal signal and two external video inputs(one switchable for CVBS or Y/C).
  - The output signal of the video source select is externally available (also as CVBS when Y/C input is used).
  - External audio input.
  - Linear RGB input with fast blanking.
- **Synchronization and Deflection**
  - Horizontal synchronization with two control loops and alignment free horizontal oscillator.
  - Slow start and slow stop of the horizontal drive output to enable low stress start-up and switch-off from the line circuit at nominal line supply voltage.
  - Vertical count-down circuit for stable behavior with provisions for non-standard signals.
  - Vertical geometry control.
  - Vertical drive optimized for DC coupled vertical output stages.
- **Control**
  - Full I2C bus control, as well for customer controls as for factory alignment.
  - All automatic controls have an option for forced mode.
- **Power consumption**
  - Low power consumption (900 mW at 8.0 Volts).
- **Packaging**
  - SDIL-56 (Shrinked Dual In Line, 56 pins).

(3) Block Diagram



No	Name	Description
1	SOUND IF INPUT	not used.
2	EXT AUDIO INPUT	not used.
3 4	VCO REF FILTER	The IF VCO tuned circuit is applied to these pin. Its resonance frequency must be two times the IF-frequency and in between a range of 64-120MHz. This range is suitable for the IF standards as 33.4, 38.9, 45.75 and 58.75MHz. The VCO frequency can be adjusted by I2C bus so a fixed coil can be used.
5	PLL LOOP FILTER	The PLL loopfilter is a first order filter with R=390 ohm and C = 100nF in series to ground. The loopfilter bandwidth is 60kHz and is optimal for both fast catching and sufficient video suppression for optimal sound performance. Sound performance can theoretically be improved by adding a small capacitor (approx.0- 4.7nF) between pin 5 and ground. This however must be evaluated further because the normal video signal response should not be effected.
6	IF VIDEO OUTPUT	Although the video output impedance is low it is recommended to avoid high frequency current in the output due to for instance sound trap filters. This can be achieved by means of an emitter follower at the video output with a 1 kΩ resistor in series with the base.
7	BUS INPUT : SCL	Serial clock line
8	BUS INPUT : SDA	Serial data line
9	BANDGAP DECOUPLING	The bandgap circuit provides a very stable and temperature independent reference voltage. This reference voltage (6.7V) ensures optimal performance of the TDA8375 and is used in almost all functional circuit blocks.
10	CHROMA INPUT	The supplied C S-VHS input burst amplitude should be nominally 300mVpp (assumed is a colour bar signal with 75% saturation and with chroma/burst ratio of 2.2/1). The C S-VHS input is internally clamped to 4V via 50 kΩ. The external AC coupling capacitor with 50 kΩ forms a high pass filter. A recommended coupling capacitor is 1 nF; the high pass filter cut off frequency is then approximately 3KHz.
11	Y/CVBS INPUT	The Y S-VHS signal of 1Vpp (inclusive sync amplitude) is AC coupled to pin11.
12 37	MAIN POSITIVE SUPPLY	The TDA8375 has a main supply pin 12 and a horizontal supply pin 37. Both pins have to be supplied simultaneously. Notice that the IC has not been designed to use this pin 37 as start pin. (pin 37 supplies the horizontal oscillator, PHI-1 and PHI-2) (pin 12 supplies the rest of the circuits in the IC) The nominal supply voltage is 8V. With min/max values of 7.2-8.8V. Also in stand-by condition the IC must be supplied with 8V. A voltage detection circuit is connected to both pins. - pin12 if V12 <6.8V than a power on reset, POR, is generated. The Hout output is disabled immediate. - pin37 if V37 <5.8V than the horizontal output is disabled immediate.

No	Name	Description
13 17	INT CVBS INPUT EXT CVBS INPUT	It is recommended that the CVBS1 int and CVBS2 ext input amplitudes are 1 Vpp (inclusive sync amplitude). This, because the noise detector switches the ϕ1 loop to slow mode (i.e. auto ϕ1mode when FOA, FOB = 0,0) when noise level exceeds 100mVrms (i.e. at S/N of 20dB).
14	GROUND	All internal circuits are connected to this ground pin 14.
15	AUDIO OUTPUT	not used.
16	DECOUPLING FILTER TUNING	Voltage variations at pin 16, which can be due to external leakage current or crosstalk from interference sources, should be less than 50mV to ensure that tuning of filters/delay cells remains correct.
18	BLACK CURRENT INPUT	For correct operation of the loop CURRENT information is supplied to the black current input pin.
19 20 21	BLUE OUTPUT GREEN OUTPUT RED OUTPUT	The RGB outputs are supplied to the video output stages from pins 21, 20 and 19 respectively. For nominal signals (i.e. CVBS/S-VHS, -(R-Y)/- (R-Y), TXT inputs) and for nominal control settings, then the RGB output Signal amplitudes is typically 2VBLACK_WHITE.
22	V-GUARD INPUT/ BEAM CURRENT LIMITER	**Vertical Guard** With this function, the correct working of the vertical deflection can be monitored. If the vertical deflection fails, the RGB outputs are blanked to prevent damage to the picture tube. **Beam current limiting** The beam current limiting function is realised by reducing the contrast (and finally the brightness) when the beam current reaches s too high level. The circuit falls apart in two functions: - Average beam current limiting (ABL): reacting on the average content of the picture - Peak white limiting (PWL): reacting on high local peaks in the RGB signal.
23 24 25	RED INPUT GREEN INPUT BLUE INPUT	The Rin, Gin, Bin input signals (nominal signal amplitude of 700mV) are AC coupled to pin 23, 24 and 25 respectively. Clamping action occurs during burstkey period.
26	RGB INSERTION SWITCH INPUT	The table below a survey is given of the three modes which can be selected with a voltage on RGB insertion switch input pin ; Vpin26 I2C function Selected RGB signal 0.9V-3V IE1=0 RGB(internal) IE1=1 Rin,Gin,Bin (fast insertion on pin23,24,25) > 4V IE1=X OSD can be inserted at the RGBout pins
27	LUMINANCE INPUT	An nominal input signal amplitude of 1 Vblack-white MUST be DC coupled to the luminance input pin 27. The pin is internally AC coupled to the luminance clamp via a capacitor of 50pF; clamping action occurs during burstkey period.
28	LUMINANCE OUTPUT	The luminance output signal is approximately I V black-white with typical output impedance of 25O ohm.

No	Name	Description
29 30	B-Y OUTPUT R-Y OUTPUT	The maximum output impedance of pins 29 and 30 is 500 Ω when PAL/NTSC signals are identified. When SECAM is identified by the SECAM add-on and no PAL/NTSC is already identified by the ASM, then the ASM sets the -(B-Y)/-(R-Y) output switch open (via DEMSW). This enables the -(B-Y)/-(R-Y) outputs of the TDA8395 to be directly connected to pins 29 and 3O respectively.
31 32	B-Y INPUT R-Y INPUT	The -(B-Y),-(R-Y) output signals (supplied from baseband delay line) are AC coupled, via a coupling capacitor of 10nF or greater, to the -(B-Y)/-(R-Y) inputs; both inputs are clamped during burstkey period.
33	SECAM REF OUTPUT	The SECAM reference output is directly connected to pin I of the TDA8395 for SECAM decoding ; it also can be used as a reference for comb filter applications.
34 35	X-TAL 3.58 X-TAL 4.43	To ensure correct operation of both: - colour processing internal circuits, - sync calibration internal circuits, it is only allowed to have 3.6MHz Xtals on pin34: both 4.4MHz,3.6MHz Xtals are allowed on pin 35. If pin 35 is not used: then it is left open in application (also XA,XB=O,1).
36	LOOP FILTER BURST PHASE DETECTOR	One of the important aspects of the PLL is the 1oop filter connected to pin 36; it influences the dynamic performance of the loop.
38	CVBS OUTPUT	The output amplitude is 1Vpp (transfer gain ratio between CVBS1int or CVBS2ext or CVBS3ext/Ys-vhs and CVBSout is 1). The maximum output impedance is 250 ohm.
39	BLACK PEAK HOLD CAPACITOR	For the correct working of the black stretcher an external time constant should be added at the black peak hold capacitor input.
40	HOR OUTPUT	This open collector output is meant to drive the horizontal output stage. The output is active low, i.e. the line transistor should conduct during the low period of the output.
41	SANDCASTLE OUTPUT/ FLYBACK INPUT	Pin 41 is a combined input/output pin. The pin provides a three level sandcastle pulse. Both burstkey pulse and vertical blanking pulse are always available, the line blanking pulse is only present when the external flyback pulse is fed to this pin. The line flyback pulse, fed to this pin is used for two functions: - input signal for the PHI-2 1oop and - RGB line blanking. (without flyback pulse blanking occurs only during the burstkey pulse) To ensure correct working of the delay line and SECAM add-on, the output should not be loaded with more than: - Sandcastle input delay line TDA 4665 - Sandcastle input SECAM add-on TDA 8395
42	PHI-2 FILTER / FLASH PROTECT	The loopfilter is a first order filter. This pin requires a capacitor (C) only. A flash protection becomes active when this pin is forced >6V. The horizontal drive is switched-off immediately. Once the voltage is <6V the horizontal drive is switched-on again via the slow start procedure.

No	Name	Description
43	PHI-1 FILTER	The loopfilter connected to pin 43 is suitable for various signal conditions as strong/weak and VCR signal. This is achieved by switching of the loopfilter time constant by changing the PHI-1 output current. Via I2C bus FOA/B, different time constants can be chosen, including an automatic mode which gives optimal performance under varying conditions.
44	GROUND	To this pin are connected the IC-substrate and horizontal output.
45	EAST-WEST DRIVE	The EW drive is a current output. The output is single-ended and is fed directly to the EW-input terminal
46 47	VERT DRIVE + VERT DRIVE -	The vertical drive has a current output. The output is balanced which ensures a good common mode behavior with temperature and makes the output signal less sensitive for disturbances.
48 49	IF INPUT	The PLL frequency range is 32-60MHz with corresponding VCO frequency 64-120MHz. The IF input impedances is 2 kΩ in parallel with 3pF and matches the required load for commonly used SAW filters. A DC coupling is allowed, so no series capacitors between SAW filter and IF input are necessary.
50	EHT/OVERVOLTAGE PROTECT INPUT	The input range for EHT tracking is 1.2 ~ 2.8V, for a compensation of +/- 5% on vertical and/or EW. The tracking on EW can be switched on/off by HCO. The overvoltage protection is activated when the voltage on pin 50 exceeds 3.9V typical.
51	VERT SAWTOOTH CAPACITOR	This pin requires a capacitor to ground of I00nF +/- 5%. The optimal sawtooth amplitude is 3.5V and is determined by the external capacitor and charge current. The sawtooth bottom-level is 2V.
52	REFERENCE CURRENT INPUT	This pin requires a resistor to ground. The optimal reference current is 100 μA. which is determined by this resistor.
53	AGC DECOUPLING CAPACITOR	The AGC capacitor value is 2.2 μF and has been defined for an optimal compromise between AGC speed and tilt for all AGC modes (negative/positive modulation).
54	TUNER AGC OUTPUT	This output is used to control (reduce) the tuner gain for strong RF signals. The tuner AGC is an open collector output which is acting as a variable current source to ground.
55	AUDIO DEEMPHASSIS	not used.
56	DECOUPLING SOUND DEMODULATOR	This pin requires a capacitor of 10 μF connected to ground. The pin acts as a low pass filter needed for the DC feedback loop.

TDA4665(Base Band Delay Line)

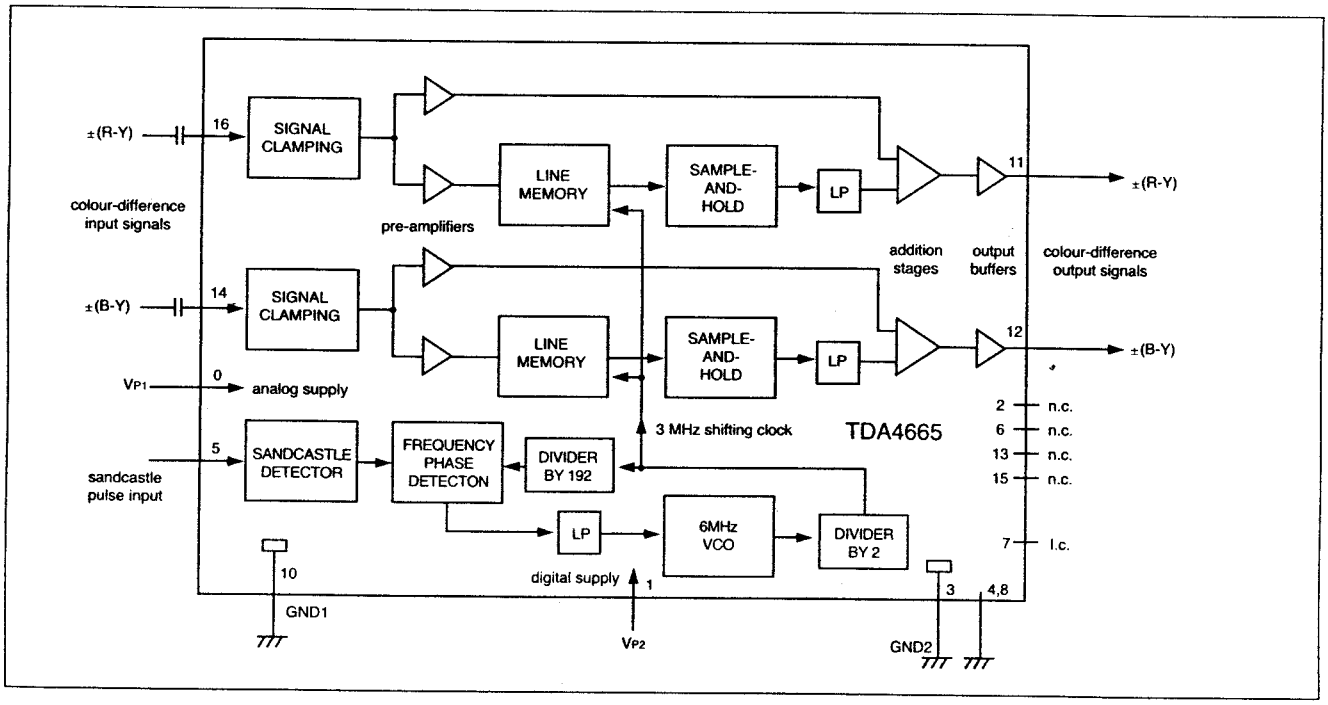
(1) Features

- Two comb filters, using the switched-capacitor technique,for one line delay time (64μs)
- Adjustment free application
- No crosstalk between SECAM colour carriers
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals(±(R-Y)and±(B-Y))
- VCO without external components
- 3MHz internal clock signal derived from a 6MHz VCO, line-locked by the sandcastle pulse (64μs line)
- Sample-and -hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour

(2) General Description

The TDA4661 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs±(R-Y)and±(B-Y).

(3)Block Diagram



(4) Pin Description

SYMBOL	PIN	DESCRIPTION
V_{p2}	1	+5V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected

SYMBOL	PIN	DESCRIPTION
V_{p1}	9	+5V supply voltage for analog part
GND1	10	ground for analog part (0V)
V_o(R-Y)	11	± (R-Y) output signal
V_o(B-Y)	12	± (B-Y) output signal
n.c.	13	not connected
V_i(B-Y)	14	± (B-Y) input signal
n.c.	15	not connected
V_i(R-Y)	16	± (R-Y) input signal

TDA8395 (Secam Decoder)

(1) Features

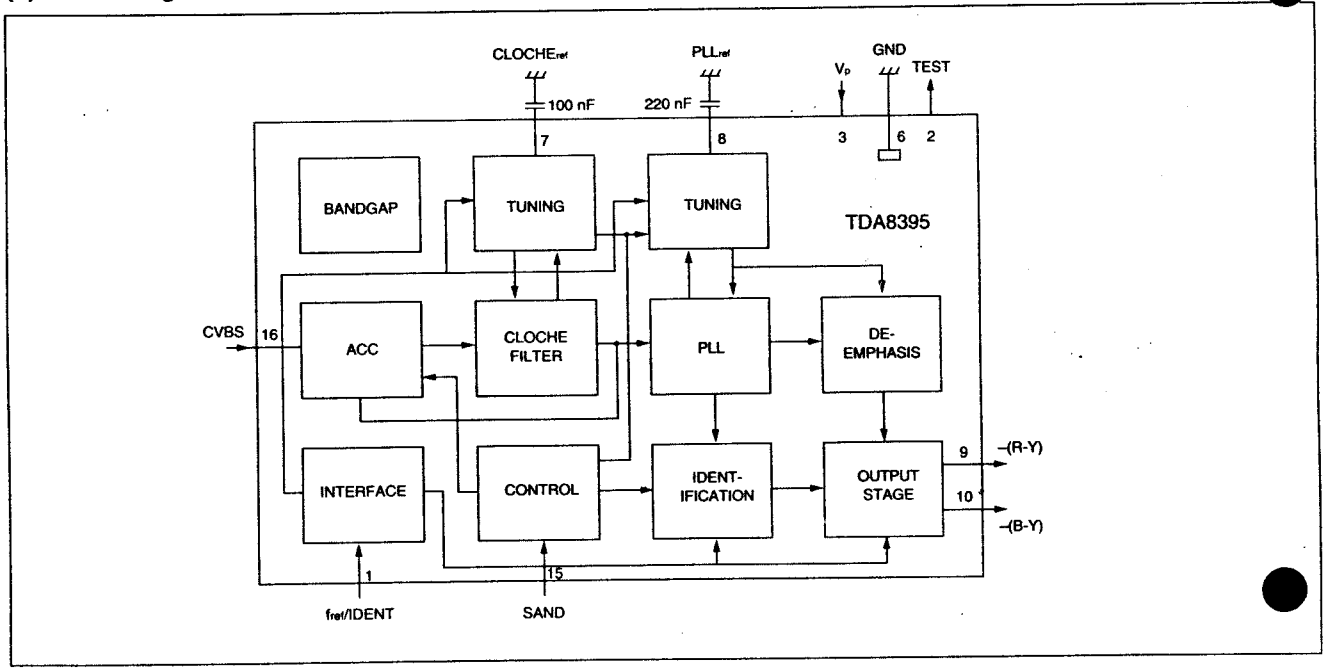
- Fully integrated filters
- Alignment free
- For use with baseband delay

(2) Description

The TDA8395 is a self-calibrating,fully integrated SECAM decoder. The IC should preferably be used in conjunction with the PAL/NTSC decoder TDA8362 and with the switch capacitor baseband delay circuit TDA4665. The IC incorporates HF and LF filters, a demodulator and an identification circuit (luminance is not processed in this IC).

A highly stable reference frequency is required for calibration and a two-level sandcastle pulse for blanking and burst gating.

(3) Block Diagram



(4) Pin Description

SYMBOL	PIN	DESCRIPTION
fp1/IDENT	1	reference frequency input/identification input
TEST	2	test output
Vp	3	positive supply voltage
n.c.	4	not connected
n.c.	5	not connected
GND	6	ground
CLOCHEref	7	Cloche reference filter
PLL ref	8	PLL reference
-(R-Y)	9	-(R-Y) output
-(B-Y)	10	-(B-Y) output
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
SAND	15	sandcastle pulse input
CVBS	16	video (chrominance) input

TDA6106Q (Video Output Amplifier)

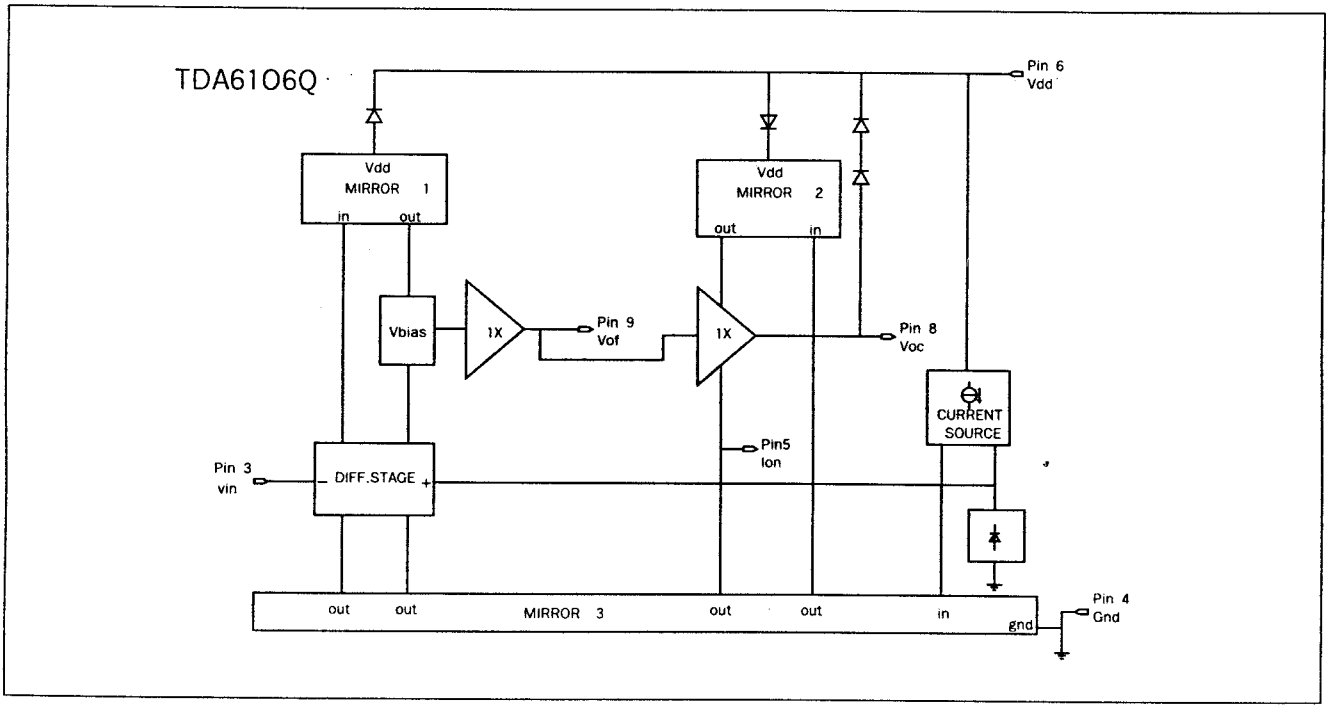
(1) General Description

The TDA6106Q is a monolithic video output amplifier (5MHz bandwidth) in a SIL 9 MPpackage, using high-voltage DMOS technology, and is intended to drive the cathode of CRT directly .
To obtain maximum performance, the amplifier should be used with black-current control.

(2) Feature

- Black - current measurement output for automatic black current stabilization (ABS)
- Single supply voltage of 200V
- Internal protection against positive appearing CRT flash-over discharge
- Protection against ESD
- Internal 2.5V reference circuit
- Controllable switch-off behavior

(3) Block Diagram



(4) Pin Description

PIN	SYMBOL	DESCRIPTION
1		N.C
2		N.C
3	V in	inverting input
4	GND	ground, substrate
5	I om	Black-current measurement output
6	V dd	supply voltage high
7		N.C
8	V oc	cathode output
9	V of	feedback/transient output

TDA8351 (DC-coupled vertical deflection circuit)

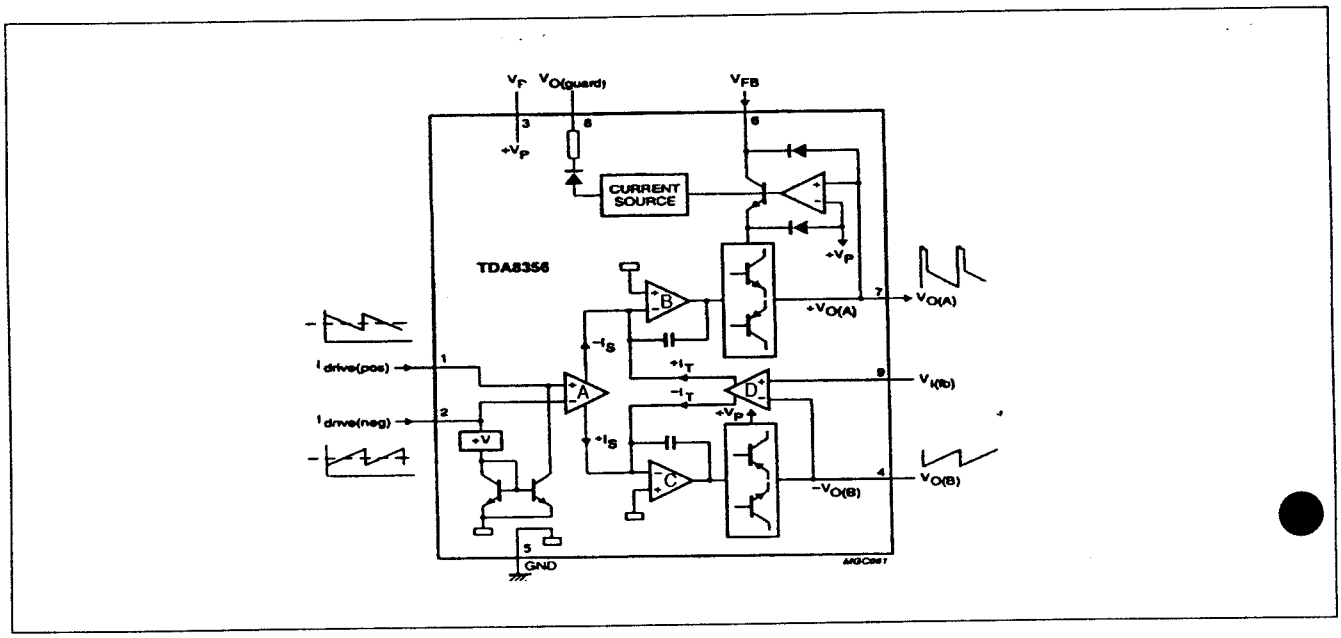
(1) General Description

The TDA8351 is power circuit for use in 90° and 110° color deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a high efficient class G system.

(2) Feature

- High efficient fully DC-coupled vertical output bridge circuit
- Vertical fly-back switch
- Guard circuit
- Protection against : - short circuit of the output pins (7 and 4)
  - short circuit of the output pins to Vp
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

(3) Block Diagram



(4) Pin Description

PIN	SYMBOL	DESCRIPTION
1	I drive (pos)	input power stage (positive); include Ii(sb) signal bias
2	I drive (neg)	input power stage (negative); include Ii(sb) signal bias
3	V p	operating supply voltage
4	V o(b)	output voltage B
5	GND	ground
6	V fb	input fly-back supply voltage
7	V o(a)	output voltage A
8	V o(guard)	guard output voltage (Not used)
9	V I(fb)	input feedback voltage

STR-S5707 (Hybrid IC for a Switching Regulator)

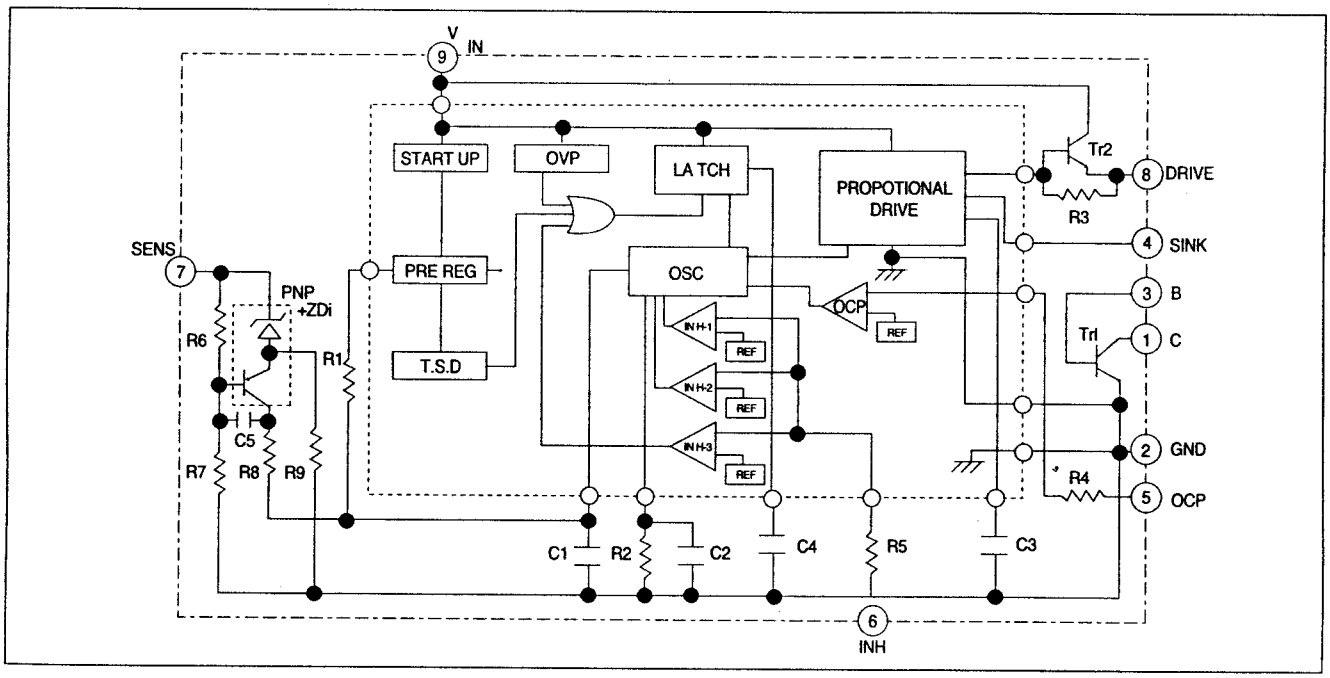
(1) General Description

The STR-S5707 is a Hybrid IC with a built in power transistor and a separate excitation control IC, designed for converter type switching mode power supply applications.
The IC is capable of quasi-resonant mode and requires small number of external component.

(2) Feature

- Small SIP isolated package : Resin sealed type (transfer mold)
- Lower power dissipation at a lighter load
- Many protection function : - Pulse-by-pulse over current protection
  - Over-voltage protection with a latch
  - Thermal protection with a latch
- These protection functions are incorporated and can be latched with an external signal.

(3) Block Diagram



(4) Pin Description

PIN	NAME	SYMBOL	DESCRIPTION
1	Collector	C	Collector of power Tr
2	Ground	GND	ground (Emitter of power Tr)
3	Base	B	Base of power Tr
4	Sink	SINK	Base current (IS) input
5	Over-current protection	OCP	over-current sensing signal input
6	Inhibit Latch	INH	input for synchronizing OFF time and latch circuit operation
7	Sensing	SENS	constant voltage control signal input
8	Drive	DRIVE	Base drive current (ID) output
9	Vin	VIN	supply voltage for control circuit

Electrical Characteristics of Control Part (Ta=25℃)

Description	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
On-state Voltage	9-2	$V_{IN(ON)}$	7.6	8	8.4	V
Off-state Voltage	9-2	$V_{IN(OFF)}$	4.6	4.9	5.2	V
Operating Circuit Current	9-2	$I_{IN(ON)}$	15	—	28	mA
Stand-by Circuit Current	9-2	$I_{IN(OFF)}$	—	—	200	μA
On Time	—	T_{ON}	33	—	41	μsec
Off Time	—	T_{OFF}	45	—	55	μsec
OCP terminal Threshold Voltage	6-2	V_{OCP}	-1.12	-1	-0.88	V
INH terminal Threshold Voltage 1	8-2	V_{INH-1}	0.65	0.75	0.85	V
INH terminal Threshold Voltage 2	8-2	V_{INH-2}	—	1.4	2..0	V
INH terminal Threshold Voltage 3	8-2	V_{Latch}	3.2	5.1	5.8	V
OVP Operating Voltage	9-2	$V_{IN(OVP)}$	9.2	—	10.7	V
Latch Circuit Sustaining Current	9-2	I_H	—	—	500	μA
Latch Circuit Cancellation Voltage	9-2	$V_{IN(La.OFF)}$	2.5	3.1	—	V
MIC Thermal Shutdown Starting Temp	—	$T_{j(TSD)}$	125	150	—	℃
Fixed Reference Voltage	7-2	V_S	32.0 ±0.3			V
Temperature Coefficient of Reference Voltage	7-2	—	—	+2.5	—	mV/℃

Electrical Characteristics of Power Transistor Part(Trl) (Ta=25℃)

Description	Terminal	Symbol	Rating			Unit
			MIN	TYP	MAX	
Collector Saturation Voltage	1-2	$V_{CE(sat)}$	—	—	0.4	V
Collector Cutoff Current	1-2	I_{CEX}	—	—	100	μA
Base-Emitter saturation voltage	3-2	$V_{BE(sat)}$	—	—	1.5	V
DC Current Gain	—	h_{FE}	29	—	61	—
Thermal Resistance	—	θj-F	—	—	1.3	℃/W
Switching Time	1-2	ts	—	—	15	μsec
	1-2	tf	—	—	0.5	

TDA8138 (5.1V+12V regulator with Disable and Reset)

(1) General Description

The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

A internal reset cuicuit generates a reset pulse when the output 1 decrease below the regulated voltage value.

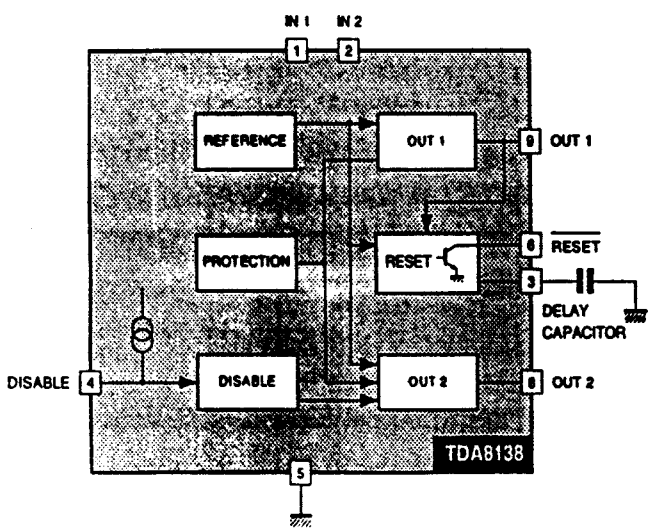
Output 2 can be disabled by TTL input.

Shot circuit and themal protections are included.

(2) Feature

- output currents up to 1A
- ixed precision Output 1 voltage 5.1V ±2%
- fixed precision Output 2 voltage 12V ±2%
- output 1 with Reset facility
- output 2 with Disable by TTL input
- short circuit protection at both outputs
- thermal protection
- low drop output voltage

(3) Block Diagram



(4) Pin Description

PIN	SYMBOL	DESCRIPTION
1	V in 1	input 1
2	V in 2	input 2
3	C e	Delay capacitor
4	V dis	disable
5	GND	ground
6	RST	reset
7		n.c
8	V out 2	output 2 (12V)
9	V out 1	output 1 (5.1V)

TDA1519B (BTL or STEREO audio amplifier)

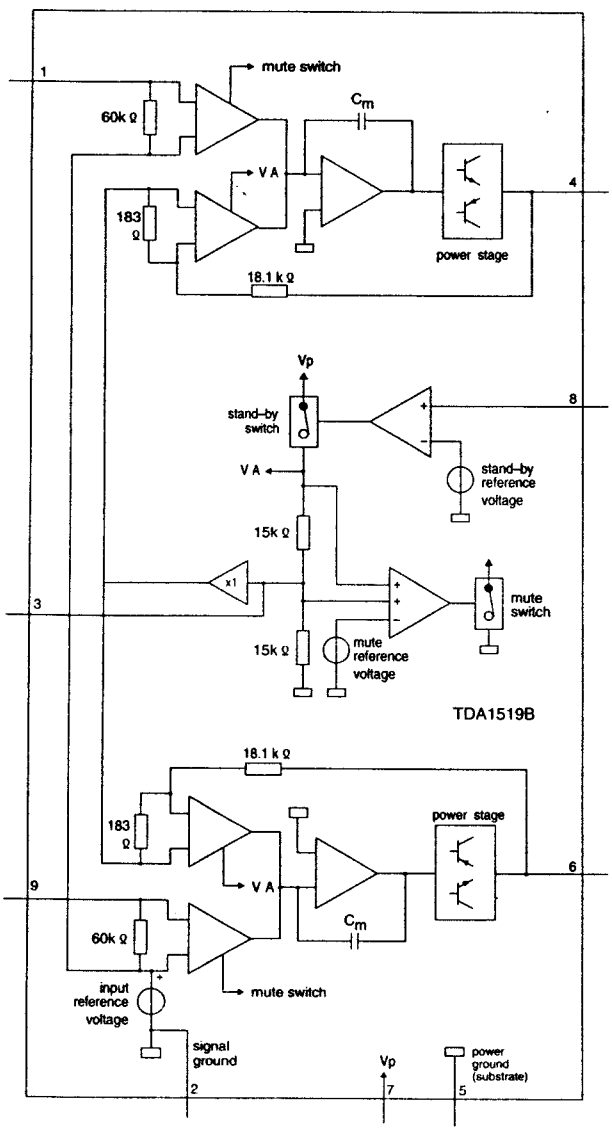
(1) Features

- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- SC and DC short-circuit-safe to ground and VP
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (VP = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519A (except output power)

(2) General Description

The TDA1519B is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

(3) Block Diagram



(4) Pin Description

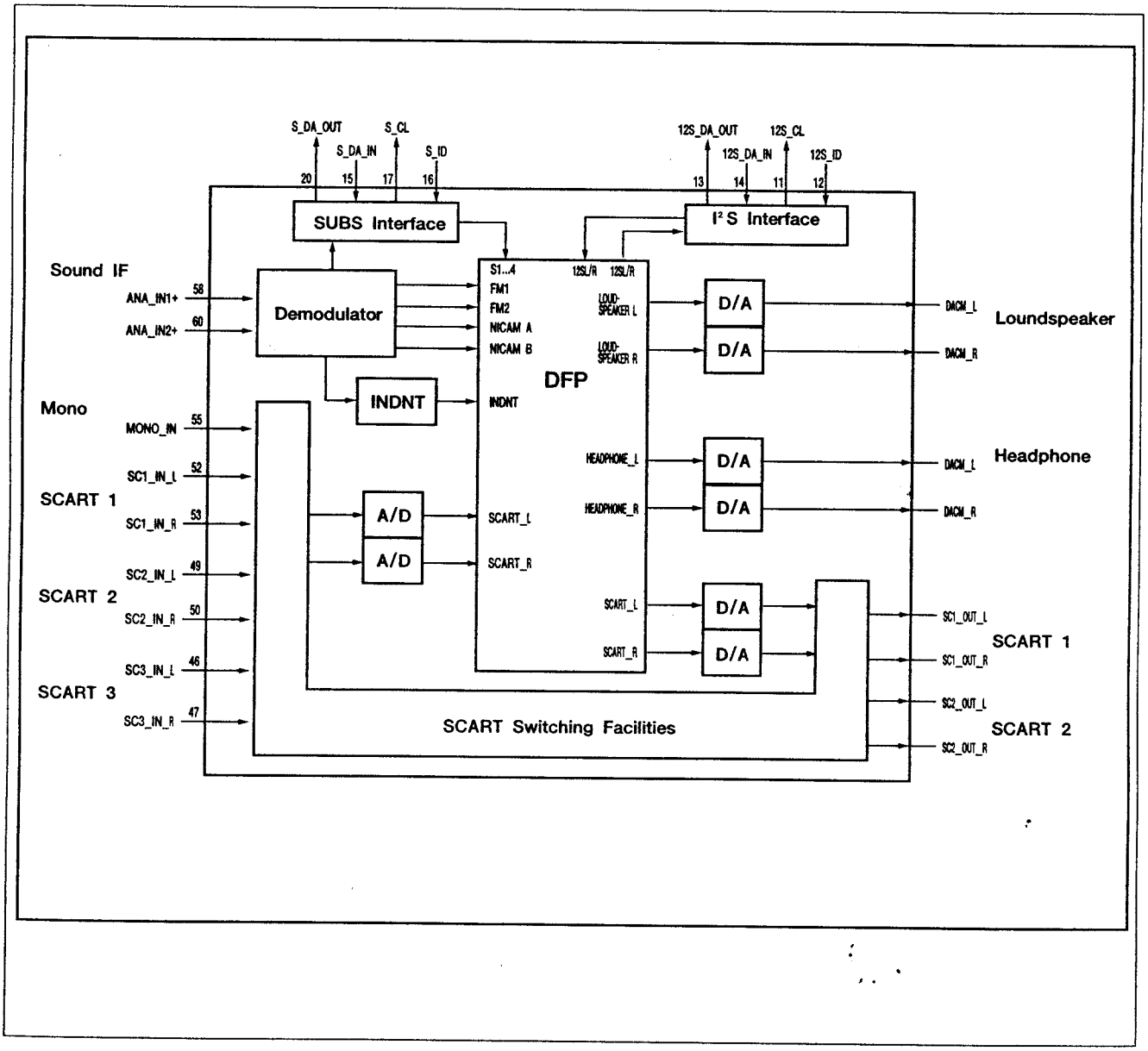
PIN	NAME	DESCRIPTION
1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	Vp	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

MSP3410 (Multistandard Sound processor for NICAM & 2-Carrier

(1) Features

- Asingle-chip Multistandard Sound Pressor for applications in analog and digital TV sets
- TWO selectable analog inputs
- Automatic Gain control for analog input
- All demoudlation and filtering is performed on chip and is individually programmable
- Adjustment of volume, balance, loudness, treble, bass, base width enlargement, pseudo stereo
- Independent input selection for speaker-out and scart-out

(2) Block Diagram



(3) Description

• Analog Sound IF - Input Section

The input pins ANA_IN1+, ANA_IN2+ and ANN_IN-offer the possibility to connect two different sound IF sources to the MSP 3410. By means of bit [8] of AD_CV either terrestrial or satellite sound IF signals can be selected. The analog-to-digital conversion of the preselected sound IF signal is done by a flash-converter, whose output can be used to control an analog automatic gain circuit (AGC), providing optimum level for a wide range of input levels. It is possible to switch between automatic gain control and a fixed (setable) input gain. In the optimum case, the input range of the AD converter is completely covered by the sound if source. Some combinations of SAW filters and sound IF mixer IC's however show large picture components on their outputs. In this case filtering is recommended. It was found, that the high pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ are sufficient in most cases.

• Quadrature Mixers

The digital input coming from the integrated A/D converter may contain audio information at a frequency range of theoretically 0 to 9 MHz corresponding to the selected standards. By means of two programmable quadrature mixers two different audio sources, for example NICAM and FM-mono, may be shifted into baseband position. In the following the two main channels are provided to process either:

- NICAM (channel 1) and FM mono (channel 2) simultaneously or alternatively

- FM2 (channel 1) and FM1 (channel2).

Two independent digital oscillators are provided to generate two pairs of sin/cos-functions. Two programmable increments, to be divided up into Low- and High part, determine frequency of the oscillator, which corresponds to the frequency of the desired audio carrier.

• Lowpass Filtering Block for Mixed Sound IF Signals

By means of decimation filters the sampling rate is reduced. Then, data shaping and/or FM bandwidth limitation is performed by a linear phase Finite Impulse Response (FIR-filter). Just like the oscillators' increments the filter coefficients are programmable and are written into the IC by the CCU via the control bus. Thus, for example, different NICAM versions can easily be implemented. Two not necessarily different sets of coefficients are required, one for channel 1 (NICAM or FM2) and one for channel 2 (FM1=FM-mono).

Since both MSP channels are designed to process the German FM Stereo System with the same FIR coefficient set (despite 7 dB power level difference of the two sound carriers), the MSP channel 1 has an internal overall gain of 6 dB. To process two carriers of identical power level these 6 dBs have to be taken into account by decreasing the values of the channel 1 coefficient set.

• CORDIC Block

The filtered sound IF signals are demodulated by transforming the incoming signals from Cartesian into polar format by means of a CORDIC processor block. On the output, the phase and amplitude is available for further processing. AM signals are derived from the amplitude information whereas the phase information serves for FM and NICAM (DQPSK) demodulation.

• Differentiators

FM demodulation is completed by differentiation the phase information output of the CORDIC block.

• Lowpass Filer Block for Demodulated Signals

The demodulated FM and AM signals are further lowpass filtered and decimated to a final sampling frequency of 32 kHz. The usable bandwidth of the final baseband signals is about 15 kHz.

• DQPSK-Decoder

In case of NICAM-mode the phase samples are decoded according the DQPSK-Coding scheme. The output of this block contains the original NICAM-bitstream, which is available at the N-Bus interface.

• NICAM-Decoder

Before any NICAM decoding can start, the MSP must lock to the NICAM frame structure by searching and synchronizing to the so-called Frame Alignment Words (FAW).

To reconstruct the original digital sound samples the NICAM-bitstream has to be descrambled, deinterleaved and rescaled. Also bit error detection and correction (concealment) is performed in this NICAM specific block.

To facilitate the Central Control Unit CCU to switch the TV-set to the actual sound mode, control information on the NICAM mode and bit error rate are supplied by the the NICAM-Decoder, It can be read out via the I^2C-Bus.

• Analog Section and SCART Switches

The analog input and output sections offer a wide range of switching facilities, which are shown in Fig. To realize a TV-set with 3 pairs of SCART-inputs and two pairs of SCART-outputs no external switching hardware is required.

The switches are controlled by the ACB bits defined in the audio processing interface (see chapter "programming the audio processing part").

If the MSP 3410 is switched off by first pulling STANDBYQ low and then disconnecting the 5V but keeping the 8V power supply (**'Standby'-mode**), the switches S1, S2 and S3 maintain their position and function. This facilitates the copy from selected SCART-inputs to SCART-outputs in the TV-sets standby mode.

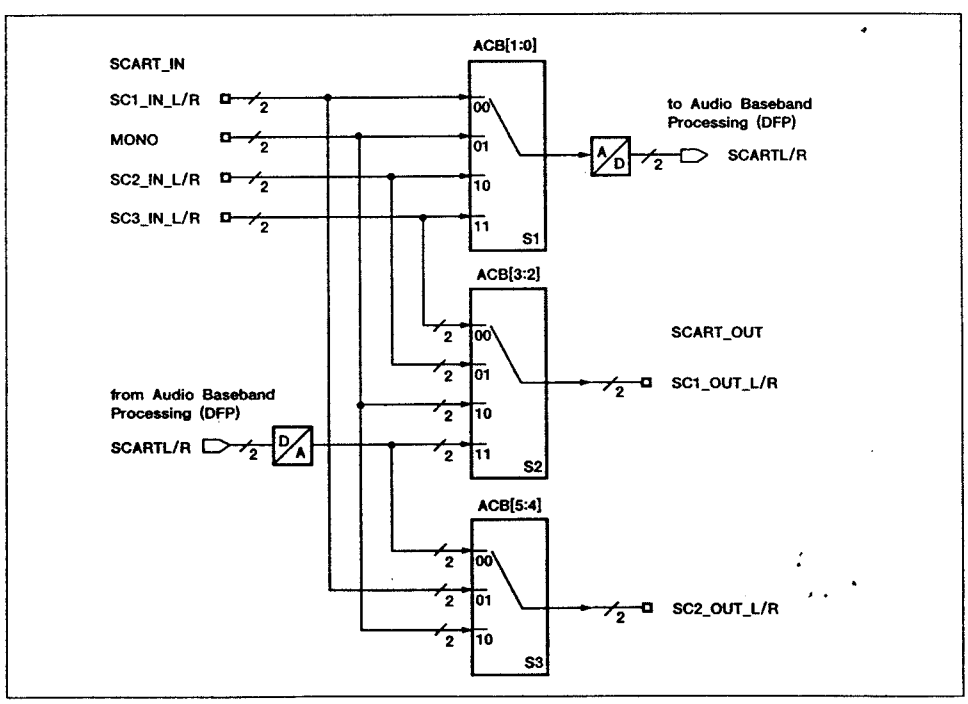


Fig. SCART-Switching Facilities Bold lines determine the default configuration

In case of power-on start or starting from standby, the IC switches automatically to the default configuration, shown in the figure above. This action takes place after the first I^2C transmission into the DFP part. By transmitting the ACB register first, the default setting mode can be changed.

• MSP 3410 Audio Baseband Processing

By means of the DFP processor all audio baseband functions are performed by digital signal processing (DSP). The DSP functions are grouped into three processing parts: Input preprocessing, channel selection and channel postprocessing.

The input preprocessing is intended to prepare the various signals of all input sources in order to form a standardized signal at the input to the channel selector. The signals can be adjusted in volume, are processed with the appropriate deemphasis and are dematrixed if necessary.

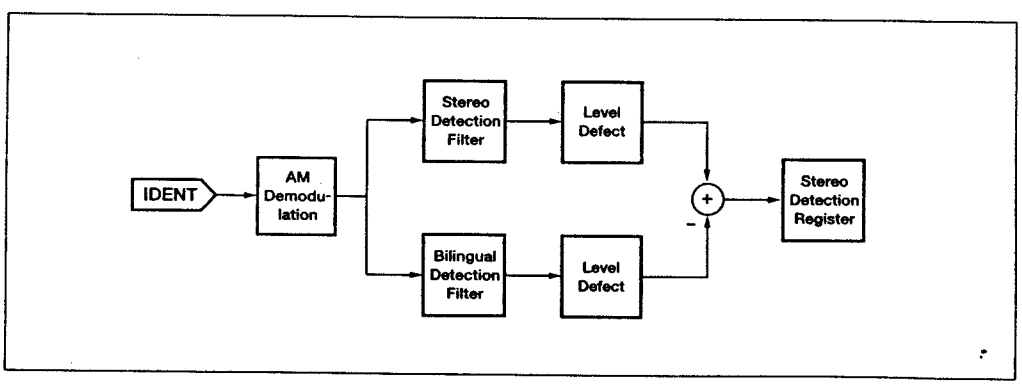
Having prepared the signals that way, the channel selector makes it possible to distribute all possible source signals to the desired output channels.

Of special importance is the ability to route in an external coprocessor for special effects like graphic equalizer, surround processing and sound field processing. Routing can be done with each input source and output channel via the I^2S inputs and outputs.

All input and output signals can be processed simultaneously with the exception that FM2 cannot be processed at the same time as NICAM. Note that the NICAM input signals are only available in the MSP 3410 version. While processing the adaptive deemphasis, no dual carrier stereo (German or Korean) or NICAM processing is possible. Identification values are not valid either.

• Dual Carrier FM Stereo/Bilingual Detection

In the German and Korean TV standard, audio information can be transmitted in three modes: Mono, stereo or bilingual. To obtain information about the current audio operation mode, the MSP 3410 detects the so-called identification signal. Information is supplied via the Stereo Detection Register to an external CCU.



(4) Pin Description

PIN	PIN NAME	DESCRIPTION
1	AUD_CL_OUT	Audio clock output
2	CW_CL	Pay-TV control clock
3	CW_DA	Pay-TV control data
4	D_CTR_OUT1	Digital control output 1
5	D_CRT_OUT0	Digital control output 0
6	ADR_SEL	Control bus address select
7	STANDBYQ	Standby (low-active)
8	D_CTR_IN 0	For future use
9	I^2C_CL	I^2C clock
10	I^2C_DA	I^2C clock
11	I^2S_CL	I^2S clock
12	I^2S_WS	I^2S wordstrobe
13	I^2S_DA_OUT	I^2S data output
14	I^2S_DA_IN	I^2S data input
15	S_DA_IN	SBUS data input
16	S_ID	SBUS ident
17	S_CL	SBUS clock
18	DVSUP	Digital power supply +5V
19	DVSS	Digital ground
20	S_DA_OUT	SBUS data output (FM/NICAM-test)
21	FRAME	NBUS frame
22	N_CL	NBUS clock
23	N_DA	NBUS data
24	RESETQ	Power-on-reset
25	DACA_R	Analog output AUX, right
26	DACA_L	Analog output AUX, left
27	VREF2	Reference ground2 high voltage part
28	DACM_R	Analog output MAIN, right
29	DACM_L	Analog output MAIN, left
30	TESTIO2	Test pin 2
31	C_DACS_R	SCART output capacitor to ground
32	C_DACS_L	SCART output capacitor to ground
33	SC2_OUT_R	SCART output2, right
34	SC2_OUT_L	SCART output2, left
35	VREF1	Reference ground1 high voltage part
36	SC1_OUT_R	SCART output, right
37	SC1_OUT_L	SCART output, left
38	CAPL_A	Volume capacitor AUX
39	AHVSUP	Analog power supply 8V
40	CAPL_M	Volume capacitor MAIN

PIN	PIN NAME	DESCRIPTION
41	AHVSS	Analog ground
42	AGNDC	Analog reference voltage high voltage part
43	PDMC1	Capacitor to BAGNDI
44	PDMC2	Capacitor to BAGNDI
45	BAGNDI	Buffered AGNDC
46	SC3_IN_L	Scart input3 in, left
47	SC2_IN_R	Scart input3 in, right
48	ASG2	Analog Shield Ground2
49	SC2_IN_L	Scart input2 in, left
50	SC2_IN_R	Scart input2 in, right
51	ASG1	Analog Shield Ground1
52	SC1_IN_L	Scart input1 in, left
53	SC1_IN_R	Scart input1 in, right
54	VREFTOP	Reference voltage IF A/D converter
55	MONO_IN	Mono input
56	AVSS	Analog ground
57	AVSUP	Analog power supply +5V
58	ANA_IN1+	IF input1
59	ANA_IN1-	IF common
60	ANA_IN2+	IF input (if ANA_IN1+is used only, connect to AVSS with 50pF Capacitor
61	TESTIO1	Test pin1
62	XTAL_IN	Crystal oscillator
63	XTAL_OUT	Crystal oscillator
64	DMA_SYNC	DMAC-sync: signal

TDA4445B (Quasi Parallel Sound Processor)

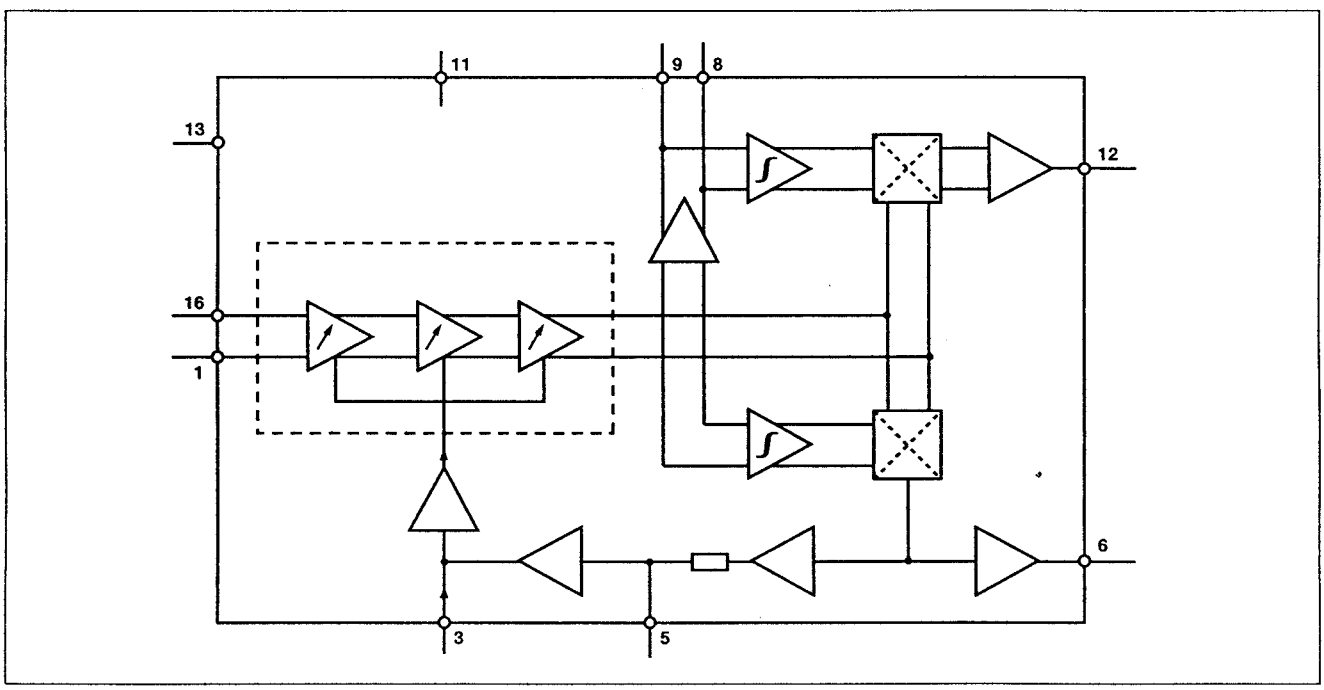
(1) Features

- Very high input sensitivity
- Excellent signal to noise ratio
- Fast averaged AGC
- IF amplifier can be switched off for VTR mode
- Output signal stabilized against supply voltage variations
- Very few external components
- Targeting bistandard applications
- Low AM distortion

(2) General Description

The TDA4445B is quasi parallel sound processor with quadrature intercarrier demodulator.

(3)Block Diagram



(4)Pin Description

PIN	DESCRIPTION
1, 16	IF input
3	IF AGC time constant
8, 9	Tuned circuit
11	Supply voltage
12	Sound-IF-output
13	Ground
2,4,7,10 14,15	not be connected
5	Average capacitor
6	AF output

GMS30112-R098 (4-bit Single Chip Microcomputer for Remote control)

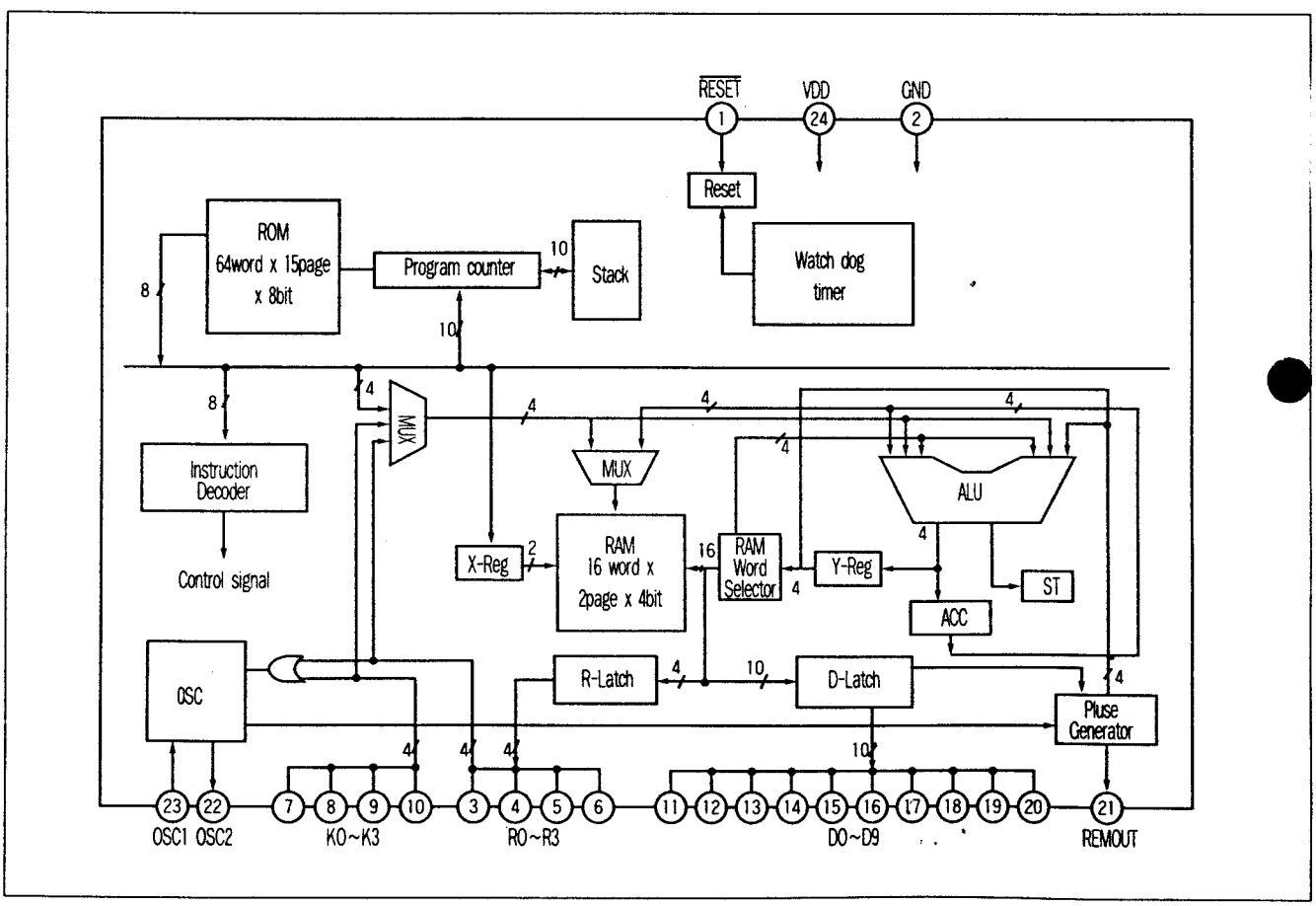
(1) General Description

The GMS30112-R098 is 4-bit single chip CMOS microcomputer.

(2) Feature

- program memory : 1024 bytes
- data memory : 32 x 4 bits
- 43 types of instruction set
- 3 levels of subroutine nesting
- 1 bit output port for a large current (REMOUT signal)
- operating frequency : 300kHz - 1 MHz
- instruction cycle : 12.5 usec @ 480kHz
- CMOS process (single 3.0 V power supply)
- stop mode (through internal instruction)
- released stop mode by key input (masked option)
- built in capacitor for ceramic oscillation circuit (masked option)
- built in a watch dog timer(WDT)
- low operating voltage (2.0 V to 4.0 V)

(3) Block Diagram



(4) Pin Description

PIN	SYMBOL	DESCRIPTION
1,2,3,4	K0,K1,K2,K3	4 bit input port with built in pull up resistor
5,6,7,8,9,10	D0,D1,D2,D3,D4,D5	10 bit output port which can be set or reset pin by pin independently. The output structure is N-channel open drain.
11	REMOUT	remote control signal output port which has high current driving capability
12	OSC 2	oscillator output
13	OSC 1	oscillator input
14	Vdd	2-4V power supply
15	RESET	reset signal input which is a low active
16	GND	ground
17,18,19,20	R0,R1,R2,R3	4 bit programmable I/O port

■ IC DC Voltage charts

* **Input signal** ..... PAL/CH5-Video : 8 step colour bar (87% AM)
  Audio : 1 KHz sinewave (60% FM)
* **User's control condition** ..... Contrast, Brightness, Colour, Volume Controls-max.
* **Line voltage** ..... AC 230V, 50Hz
* **All the voltage in each point are measured with Multimeter**.

1. TDA 8375A (I501)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	0	0	3.6	3.6	2.7	3.3	3.7	3.4	6.6	4

Pin No.	11	12	13	14	15	16	17	18	19	
V(DC)	3.5	8	4	0	3.4	3.6	3.5	5.1	3.8	3.9

Pin No.	21	22	23	24	25	26	27	28	29	30
V(DC)	4	1.9	3.5	3.5	3.5	0.3	2.8	2.8	1.8	1.8

Pin No.	31	32	33	34	35	36	37	38	39	40
V(DC)	4	4	1.6	2.6	2.6	4.9	8	8	4	1.5

Pin No.	41	42	43	44	45	46	47	48	49	50
V(DC)	0.5	4.5	4	0	0.5	2.2	2.2	4	4	1.7

Pin No.	51	52	53	54	55	56
V(DC)	3.8	3.9	3	3	3.5	3.8

2. DW 5255S * (I701)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	0	5	3.4	3.6	5	5	5	5	0	0

Pin No.	11	12	13	14	15	16	17	18	19	20
V(DC)	5	2.6	2.6	5	5	4.1	0	5	5	0

Pin No.	21	22	23	24	25	26	27	28	29	30
V(DC)	5	5	5	0	2.6	2.6	2.6	5	1.5	1.5

Pin No.	31	32	33	34	35	36	37	38	39	40
V(DC)	0.5	2.5	5	0	0	5	5	2.7	2.8	3.2

Pin No.	41	42	43	44	45	46	47	48	49	50
V(DC)	0	0	4.7	5	0.4	1.3	0	0	0	0

Pin No.	51	52
V(DC)	0	0

3. TDA 4665 (I503)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	5	0	0	0	0.6	0	0.3	0	5	0

Pin No.	11	12	13	14	15	16
V(DC)	2.9	2.9	0	1.3	0	1.3

4. TDA 4445B (I603)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	4.5	0	2.5	0	4	4	0	4.7	4.7	0

Pin No.	11	12	13	14	15	16
V(DC)	12	5.3	0	0	0	4.5

5. TDA 4445B (I602)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	4.5	0	2.6	0	4	4	0	4.8	4.8	0

Pin No.	11	12	13	14	15	16
V(DC)	12	3.7	0	0	0	4.5

6. TDA 8395 (I502)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	1.6	1.2	8	0	0	0	3.3	4.3	1.7	1.7

Pin No.	11	12	13	14	15	16
V(DC)	0	0	0	0	0.5	3.4

7. TDA 8138 (I802)

Pin No.	1	2	3	4	5	6	7	8	9
V(DC)	12	4.5	3	4.5	0	5	0	12	5

8. TDA 8351 (I301)

Pin No.	1	2	3	4	5	6	7	8	9
V(DC)	2.3	2.3	16	8.3	0	4.6	8.3	0.6	7.1

9. TDA 1519B (I601)

Pin No.	1	2	3	4	5	6	7	8	9
V(DC)	1.9	0	6.4	6.4	0	6.5	13.3	12.7	1.9

10. MSP 3410 (I602)

Pin No.	1	2	3	4	5	6	7	8	9	10
V(DC)	0	0	0	0	0	0	4.9	0	3.6	3.4

Pin No.	11	12	13	14	15	16	17	18	19	20
V(DC)	2.5	2.5	2.5	2.5	2.5	4.9	3.8	4.9	0	3.8

Pin No.	21	22	23	24	25	26	27	28	29	30
V(DC)	0	2.5	0.5	5	0.1	0.1	0	1.5	1.7	0

Pin No.	31	32	33	34	35	36	37	38	39	40
V(DC)	3.8	3.8	3.8	3.8	0	3.8	3.8	7.1	8	6.2

Pin No.	41	42	43	44	45	46	47	48	49	50
V(DC)	0	3.7	3.8	3.8	3.8	3.8	3.8	0	3.8	3.8

Pin No.	51	52	53	54	55	56	57	58	59	60
V(DC)	0	3.8	3.8	2.7	4	0	5	1.5	1.5	0.1

Pin No.	61	62	63	64
V(DC)	0	2.5	2.5	0.1

■ Circuit Description

Vision IF amplifier, AFC, video demodulator

The IF signal from the tuner is fed through a SAW filter to the differential IF input (pin 48 and 49).
The first IF stage consists of 3 AC-coupled amplifiers with a total gain control range of over 66 dB.
The reference carrier for the video demodulator is obtained by a PLL carrier regenerator
(eliminating notch filter compromises, as in reference tuned circuits for passive carrier regeneration).
Only an oscillator coil is needed(pin 3 and 4) that can be aligned via I2C-bus to the double IF frequency.

The AFC information is derived from the VCO control voltage of the IF-PLL
and can be read via I2C-bus.
Bit AFB toggles when the picture carrier is exactly at the desired IF frequency (= half the aligned IF-PLL frequency).
AFA is active in a window around this point.
For fast search-tuning applications this window can be increased by a factor 3 (AFW bit).

Tuner A.G.C.

The automatic gain control (A.G.C.) circuit operates on top sync level at negative modulated signals
or on peak white level at positive modulation, selected by MOD bit.
The tuner A.G.C. is controlled via pin 54.
The tuner A.G.C. take over point (T.O.P.) can be set over a wide range: 0.8 mVrms .. 80 mVrms
IF input signal amplitude.
The tuner AGC output may have to operate above Vcc of TDA8375A.
Therefore pin 54 is an open collector output, that can operate from 0.3 up to Vcc+ 1 Volt
(at > 2 mA sink current)

Source select switch

TDA8375A input switch can select one of the following sources ;

pin 13 front-end : CVBS I int
pin17 : CVBS 2 ext
pin 11.pinlO : Y (S-VHS), C (S-VHS)

Selected signal is available at the CVBS output pin 38, in case of Y/C input Y+C are added.
It drive teletext and the TDA8395 SECAM add-on.
For S-VHS applications, the Y,C input can be selected, independent of the CVBS source switch.
TDA8375A Y,C inputs are selected, while the source switch outputs CVBS I int or CVBS 2 ext on CVBS out.

Horizontal synchronization and protection

The synchronization separator adapts its slicing level in the middle between top-sync and black level of the CVBS signal.
The separated synchronization pulses are fed to the first phase detector and to the coincidence detector.
The ϕ-1 loop gain is determined by the components at pin 43 (C+RC).
The coincidence detector detects whether the horizontal line oscillator is synchronized to the incoming video.
The line oscillator is a VCO-type, running at twice the line frequency.
It is calibrated with the X-tal oscillator frequency of the colour decoder and has a maximum deviation of 2% of the nominal frequency, so no alignment is-needed.
Calibration is done at start up(the TDA8375A must first know what colour X-tals are connected, bits XA and XB) and after synchronization loss (ϕ-1 coincidence detector "Sync Locked" bit SL).

The second phase detector ϕ-2 locks the phase of the horizontal driver pulses at output pin 40 to the horizontal flyback pulse at input pin 41 .
This compensates for the storage time of the horizontal deflection transistor.
The ϕ- 2 loop filter (C) is externally connected to pin 42.
The horizontal phase can be given a static off set via I2C-but (HSH "horizontal shift")
A dynamic correction is possible by current feedback into the ϕ- 2 loop filter capacitor.

To protect the horizontal deflection transistor, the ho rizontal drive is switched off immediately when a power

failure (" Power-On Reset " bit POR) is detected.
The power failure may have corrupted the contents of the internal data registers, so the TDA8375A should be started up again.

The TDA8375A has a separate supply input (pin 37) that only used as a clean supply voltage for thehorizontal oscillator circuits.

Vertical synchronization

The vertical sawtooth generator drives the vertical output.
It uses an external capacitor at pin 51 and a current reference resistor at pin 52.
The TDA8375A vertical drive has differential current outputs for DC-coupled vertical output stage, like the TDA8351 .
At TDA8351 input pins I and 2 this current is converted into a drive voltage via a resistor.

Geometry processing

With the TDA8375A is possible to implement automatic geometry alignment, because all parameters are adjusted via the I2C bus.
The deflection processor of the TDA8375A offers the following five controls;

- Horizontal shift
- Vertical slope.
- Vertical amplitude
- Vertical S-correction
- vertical shift

Colour decoder

The colour decoder contains an alignment-free X-tal oscillator, a dual killer circuit and colour difference demodulators.
Together with the TDA8395 SECAM add-on a multi standard PAL/SECAM/NTSC decoder can be built with automatic recognition.
Which standard can be decoded depends on the external Xtals used.
Two Xtal pins (34and 36) are present so normally no external switching is required.
The I.C. must be told which X-tals are connected (bits XA and XB).
This is important, because the X-tal frequency of the colour decoder is also used to calibrate many internal circuit.

The burst phase detector locks the Xtal oscillator with the chroma burst signal.
The phase detector operates during the burst key period only, to prevent disturbance of the PLL by the chroma signal.
Two gain modes provide:

- Good catching range when the PLL is not Locked.
- Low ripple voltage and good noise immunity once the PLL has locked

The killer circuit switches-off the R-Y and B-Y demodulators at very low input signal conditions (chroma burst amplitude).
A hysteresis prevents on/off switching at low, noisy signals.

Color standard	pin34	pin35	XA	XB
PAL4.43/SECAM + NTSC-4.43	none	4.43	1	0
PAL4.43/SECAM + NTSC-M	3.58	4.43	1	1

Integrated video filters

The TDA8375A has alignment-free internal luminance delay, chroma bandpass and chroma trap.
They are implemented as gyrator circuits tuned by tracking to the frequency of the chroma Xtal oscillator.
The chroma trap in the Y signal path is by-passed when Y/C input is selected (S-VHS).
For SECAM an extra luminance delay is build-in, for correct delay of the luminance signal.

RGB output and black current stabilization

The colour difference signals (R-Y, B-Y) are matrixed with the luminance signal (Y) to obtain the RGBout output signals (pins 19, 20, 21).
In the TDA8375A the matrix type automatically adapts to the decoded standard (NTSC,PAL) .
Linear amplifiers are used to interface external RGB in signals (pins 23,24,25) from the SCART connector.
These signals overrule the internal RGB signals when the data insertion pin 26 (FBI) is switched to a level between 1.0V and 3.0V.

The contrast and brightness control and the peak white limiter operate on both internal and external RGB signals R,G and B each have their own, independent gain control to compensate for the difference in phosphor efficiencies of the picture tube: so called "white point" adjustment.
The nominal amplitude is about 2V black to white, at nominal input signals and control settings.

TDA8375A has a black current stabilization loop, that automatically adjust the black level to the cut-off voltage of the picture tubes three gun cathodes.
Since no current is flowing when the voltage the cathode is equal to the cut-off voltage of the tube, the loop stabilizes at a very small gun current.
This "black current" of the three guns is measured internally and compared with a reference current, to adjust the black level of RGBout.
The black level loop is active during 4 lines at the end of the vertical blanking.
In the first line the leakage current is measured (max. acceptable 100 μA).
In the next three lines the black levels of the three guns are adjusted.
The nominal value of the 'black current' is 10 μA.
The ratio of the 'black currents' for the 3 guns tracks automatically with the white point adjustment, so the back-ground colour is the same as the adjusted white point.

At switch-on of the TV receiver the black current stabilization circuit is not yet active and RGBout are blanked.
Before the first measurement pulses appear, 0.5 sec delay ensures that the vertical deflection is active, so the pulses will not be visible on the screen.
During the measuring lines RGBout will supply 4V pulses to the video output stages.
The TDA8375A waits until the black current feedback input (pin 18) exceeds 200 μA, which indicates that the picture tube is warm-up.
Then the black current stabilization circuit is active.
After a waiting time of about 1.0 sec, the blanking of RGBout is released.

Tuning

The AFC information of the TDA8375A is not available as an analogue voltage.
Automatic following (=frequency tracking, AFC) can be done via the I2C-bus by software.
The TDA8375A AFC window is typically 80 kHz wide.
This value is made higher than the 62.5 kHz tuning step, to prevent an automatic following loop from continuously adapting the tuning frequency..
With this AFC window ($\pm$40 kHz) the maximum tuning error is less than 62.5 kHz.
For high speed search-tuning-algorithms, the AFC window can be widened to 240 kHz via bit AFW.

TDA8395 SECAM decoder

The TDA8395 is an alignment-free SECAM colour decoder, including a Cloche filter, demodulator and line identification circuit.

The Cloche filter is a gyrator-capacitor type.
Its frequency is calibrated in the vertical retrace period.
The calibration reference(pin 1) is obtained from the TDA8375A color X-tal oscillator (pin 33).
Pin 7 is a decoupling for the Cloche reference.

The voltage change at this pin due to leakage currents should be lower than 10 mV, during field scan, resulting in a capacitor of minimal 100 nF.
Pin 8 is the reference capacitor for the PLL.
The voltage variation during field scan at this pin should be lower than 2 mV , resulting in a capacitor of 220 nF.

The sandcastle input (pin 15) is connected to TDA8375A pin 41 and is used for generation of the blanking periods and provides clock information for the identification circuit.
The CVBS source select output (TDA8375A pin 38) supplies SECAM chroma to pin 16 of the TDA8395.
This is demodulated by a PLL demodulator, that uses the reference frequency at pin I and a bandgap reference to obtain the desired demodulation characteristic.

If the digital line identification in theTDA8395 detects SECAM, pin 1 will sink a current of 150 (A out of TDA8375A SECAMref pin 33.
When the TDA8375A has not detected PAL or NTSC, it will respond by increasing the voltage at pin 33 from 1.5V to 5V.
Now the TDA8375A color difference outputs pin 30 and 29 are made high-ohmic and the TDA8395 output pin 9 and 10 are switched on.
These outputs will be disconnected and high-ohmic when no SECAM is detected for two frame periods, the decoder will be initialized before trying again.

SECAM-L and -L' application

For SECAM-L and L' the TDA8375A has to be switched to positive modulation via I2C-bus bit MOD.
SECAM-L' signals only occur in VHF band I and have their picture and sound carrier interchanged, compared to SECAM-L/PAL channels.

For SECAM-L' the IF picture carrier is situated at 34.5 MHz and the AM-sound carrier at 41MHz.
Therefore the IF-PLL reference has to be tuned away from 38.9 to 34.5 MHz.
This can be done via I2C-bus sub-address 15hex (IF-PLL).

The AM sound output is inserted at TDA8375A external audio input pin via the SCART plug.
When bit MOD selects positive modulation for SECAM-L/L', the TDA8375A automatically switches to external audio.

Base band delay line TDA4665

TDA4665 is an integrated double baseband delay line of 64 μS.
It couples to the TDA8375A and TDA8395 without any switches or alignments.
The TDA4665 consist of two main blocks:

- Two delay lines of 64 μsec in switched capacitor technique
- Internal clock generation of 3 MHz, line locked to the sandcastle pulse

The TDA4665 operates according to the mode demanded by the colour transmission standard:

- For PAL it operates as geometric adder to satisfy the PAL demodulation requirements
- In NTSC mode it reduces cross-colour interference (comb-filtering)
- For SECAM it repeats the colour difference signal on consecutive horizontal scan lines.

A sandcastle pulse is connected to pin 5.
The top pulse voltage (should not exceed 5 V) can be directly coupled to the 5 V sandcastle output of the TDA8375A.
The R-Y and B-Y colour difference signals (from TDA8375A pins 30 and 29) are AC-coupled and clamped by the input stages at pins 16 and 14.
An internal 6 MHz Current controlled oscillator is line locked via a PLL to the sandcastle pulse at pin 5.
This clock drives the delay lines to obtain the required 64 μsec.
Sample and hold low pass filters supress the clock signal.
The original and the delayed signals are added, buffered and fed to the output pins 11 and 12.
These are AC-coupled to the R-Y and B-Y colour difference input pin 32 and 31 of TDA8375A.

The TDA4665 needs a 5 V supply voltage on pin 1 for the digital part and on pin 9 for the analog part.

TDA8351 vertical deflection.

The TDA8351 is a vertical deflection circuit.
It can be used in 90 deflection systems with frame frequencies from 50 up to 120 Hz
With its bridge configuration the deflection output can be DC coupled with few external components.
Only a supply voltage for the scan and a second supply for the flyback are needed.
The TDA8351 can drive max.2A.

The vertical drive currents of TDA8375A pins 47 and 46 are connected to input pins 1 and 2 of the TDA8351.
The currents are converted into a voltage by a resistor between pins 1 and 2.
Pin2 is on a fixed DC level (internal bias voltage) and on pin I the drive voltage can be measured (typical 1.8 Vpp).

The drive voltage is amplified by 'A' and fed to two amplifiers 'B' and 'C', one is inverting and the other is a non inverting amplifier.
The outputs (pins 4 and 7) are connected to the series connection of the vertical deflection coil and feedback resistor .
The voltage across feed back resistor is fed via pin 9 to correction amplifier 'D', to obtain a deflection current which is proportional to the drive voltage.

The supply voltage for the TDA8351 is 16V at pin 3.
The flyback generator has a separate supply voltage of 45V on pin 6.

Horizontal deflection

The circuit contains horizontal drive, line output transformer.
The horizontal driver pulses from the TDA8375A are amplified in the horizontal drive circuit, to get sufficient base-drive current for the high voltage switching transistor Q401.
During the horizontal scan period(=52 μs) Q401 will conduct, and a sawtooth current flows from +132V through the primary winding of the FBT to ground.
After this time Q401 is switched off and the energy stored in the FBT during the scan period will be transformed to the flyback capacitor CT.
This energy transfer will take place in a cosine shape because the primary of the FBT and CT from a resonant circuit.
The time the energy is transferred from FBT to CT. and back to the FBT, is called the flyback time and will take place in about 12μs.
The flyback peak voltage is about 9 times the scan voltage.

In series with the horizontal deflection coil there is a (damped) linearity corrector coil.
During the scan there is some loss in the resistance of the deflection coil.
In the first part of a line the linearity corrector stores some energy in a permanent magnet until it is saturated.
This improves the linearity of the horizontal scan speed.
The required S correction for the picture tube can be adjusted with the value of C408.

The beam current limiting information (BeamCurr) is derived from the foot of the H.V winding of the FBT.
This is connected via resistor to +8V.
As the beam current increase, the voltage on line BeamCurr decreases.
BeamCurr is damped by a integration filter before it is fed back to TDA8375A pin 22,
The TDA8375A will decrease the contrast (and eventually the brightness) to limit the average beam current.

EW drive

The DC voltage on pin 45 is determined by the East-West driver stage input and may range from 1 to 8 volts.
To prevent distortion, the voltage must always be >1volt.
Because the DC voltage on pin 45 is equal to the minimal output voltage of the East-West driver stage (reached for i_{ew} = 0), it is recommended to choose this level close to 1 volt for maximum range.

Video amplifiers

Three TDA6106Q integrated video amplifiers drive cathode of the picture tube directly.
They are protected against CRT flashover discharges and ESD (electro static discharge).

The three video amplifiers, have a beam current output I black, used by the TDA8375A black current loop to control the black level on the cathodes.
The outputs can be connected together because the black current 100p sequentially controls the black level for each cathode.

The amplification of the TDA6106Q is set by the resistors between pin 3 and 9 and between pin 3 (negative-input) and the TDA8375A output.
There are no alignment any more on the CPT panel, because of the automatic black current stabilization and because the white point adjustment can be done in the TDA8375A via I2C bus.

Power Supply STR-S5707

(1) VIN terminal, start-up circuit

A start-up circuit is to start and stop a operation of a control IC by detecting a voltage appearing at a VIN terminal (pin-9).
At start up of a power supply, when a voltage at the VIN terminal reaches to 8V (typical) by charging up C812 by the function of a start-up resistor, R802, a control circuit starts operating by the function of the start-up circuit.
After the control circuit starts its operation, power source is obtained by smoothing voltage appearing at winding of pin6-7 of T802.

(2) Oscillator, F/B terminal voltage (Pin 7)

A oscillator generates pulse signals which turns a power transistor on and off by making use of charge and discharge of C1 and C2 incorporated in the Hybrid IC.
Constant voltage control of a switch-mode power supply is performed by changing both ON-time and OFF-time except when the load is light (ex. remote control stand-by mode of TVs).
The ON-time is controlled by changing a current charged by C1, which is as the result of that the detection winding of pin5-7 of T802, which detects a change of voltage in a secondary side, connected to the sensing terminal (Pin 7) has the current in accordance with an output signal from an output voltage detection circuit (an error amplifier) built in.
As an AC input voltage to the power supply gets the higher and a load current the smaller, the current flowing to the SENS terminal gets the larger, and the ON-time gets the shorter.

(3) Function of INH terminal (Pin 6), control of OFF-time

Signal to the INH terminal is used as inputs to COMP.1 and COMP.2 inside of the control IC.
A threshold voltage of COMP.1, VTH1 is set at 0.75V (Ta=25°) and an input signal to a drive circuit becomes almost 0V (the power transistor is in OFF mode) when a voltage at the INH terminal reaches the VTH1.
A threshold voltage of COMP.2, VTH2, is set at 1.5V (Ta=25°).
When the INH terminal voltage reaches VTH2, an output from COMP.2 reverses (the power transistor is in on mode).

* Quasi-resonant operation

By inputting the voltage of winding of pin6-7 of T802 which is synchronized with the energy discharge time of a secondary winding, pin14(or 15)-16 of T802, to the INH terminal through D805 and RC803, quasi-resonant operation can be achieved.

When the power transistor turns off and a voltage higher than VTH2 is applied to the INH terminal, C3 immediately discharges and then starts charging again.
Even after the discharge of energy of a secondary winding is completed, VINH does not immediately increases.
When it gets lower than VTH1, the transistor turns on.

* Stand-By Mode

While being in remote control stand-by mode, the output voltage is kept on providing to the secondary side and the power transistor operates at A class mode.

(4) Drive circuit

The STR-S5707 applies the proportional drive system in order to minimize turn-on and saturation loss, and storage time.

(5) OCP (over-current protection) function

Over-current protection is performed pulse by pulse by directly detecting collector current of the power transistor. Detecting voltage is set to -1V below a reference point of GND (ground).

(6) Latch circuit

It is a circuit which sustains an output from the oscillator low and stops operation of the power supply when over-voltage protection (OVP) circuit and thermal shutdown (TSD) circuit are in operation.

As the sustaining current of the latch circuit is 500 μA maximum when VIN terminal voltage is 4V, the power supply circuit sustains the off state as long as current of 500 μA minimum flows to V_{IN} terminal from a start-up resistor.

In order to prevent a malfunction to be caused by a noise and so on, delay time is provided by C1 incorporated in the IC and, therefore, the latch circuit operates when the OVP or TSD circuit is in operation, or an external signal input is provided for about 10 μsec or longer.

In addition, even after the latch circuit start operating, the constant voltage regulator (Reg) circuit is in operation and the circuit current is at high level.

As a result, V_{IN} terminal voltage rapidly decreases.

When VIN terminal voltage becomes lower than the shutdown voltage, $V_{IN(OFF)}$ (4.9V typical), it starts increasing as the circuit current is below 500 μA.

When it reaches the ON-state voltage, $V_{IN(ON)}$ (8V typical), VIN terminal voltage starts decreasing because the circuit current increases again.

When the latch circuit is on, VIN terminal voltage increases and decreases within the range from 4.9V typical to 8V typical and is prevented from abnormally rising.

Cancellation of the latch is done by decreasing VIN terminal voltage below 3.3V.

The power supply can be restarted after disconnecting an AC input to the power supply once.

(7) Thermal shutdown circuit

It is a circuit to trigger the latch circuit when the frame temperature of the IC exceeds 150°C (typical).

Although the temperature is actually sensed at the control chip, it works against overheating of the power transistor as the power transistor and the control IC are mounted on the same lead frame.

(8) Over-voltage protection circuit

It is a circuit to trigger the latch circuit when VIN terminal voltage exceeds 11V (typical).

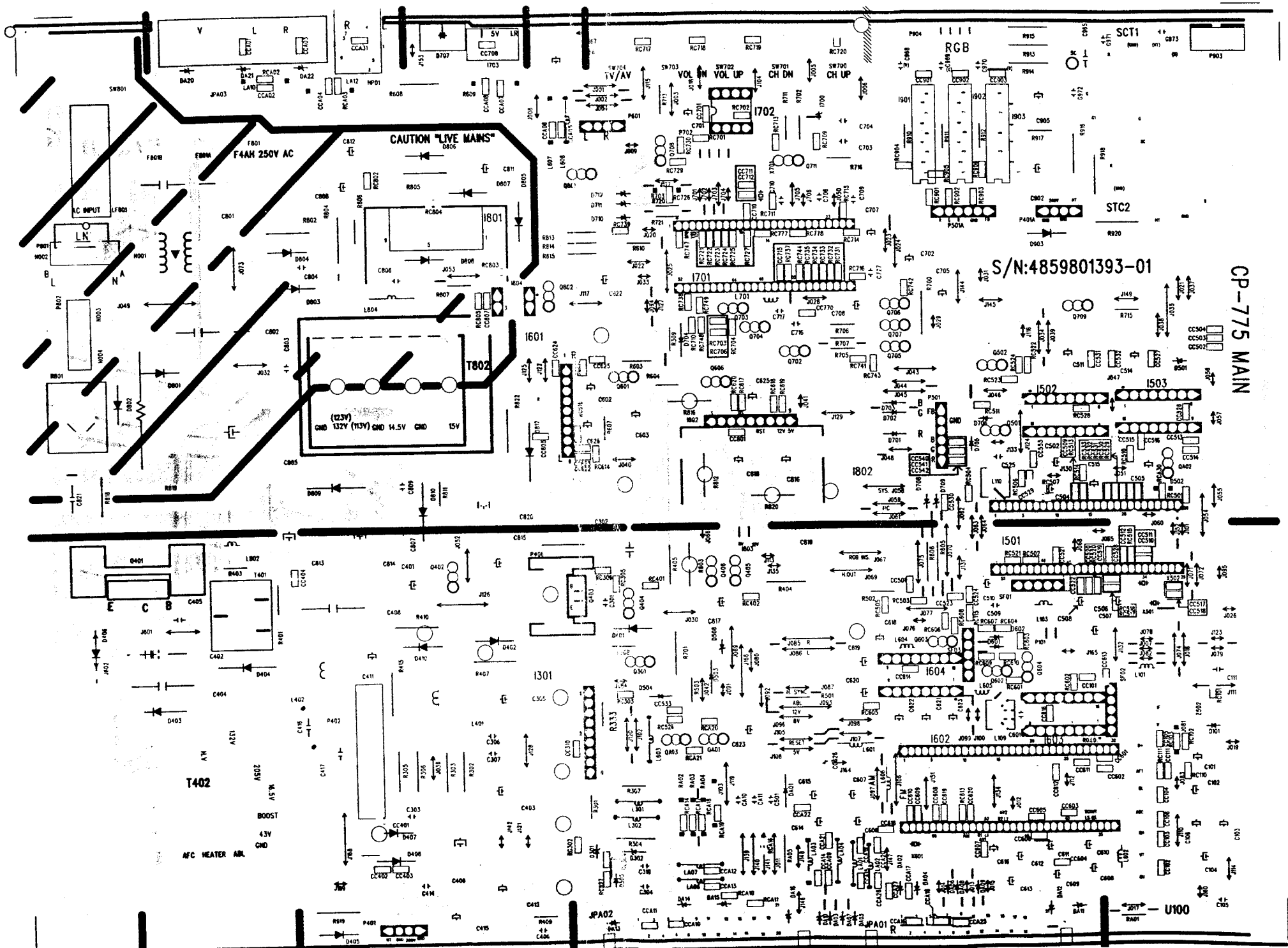
Although it basically functions as protection of VIN terminal against over-voltage, since VIN terminal is usually supplied from the drive winding of the transformer and the voltage is proportional to the output voltage, it also functions against the over-voltage of secondary output which causes when the control circuit opens or in some other events.

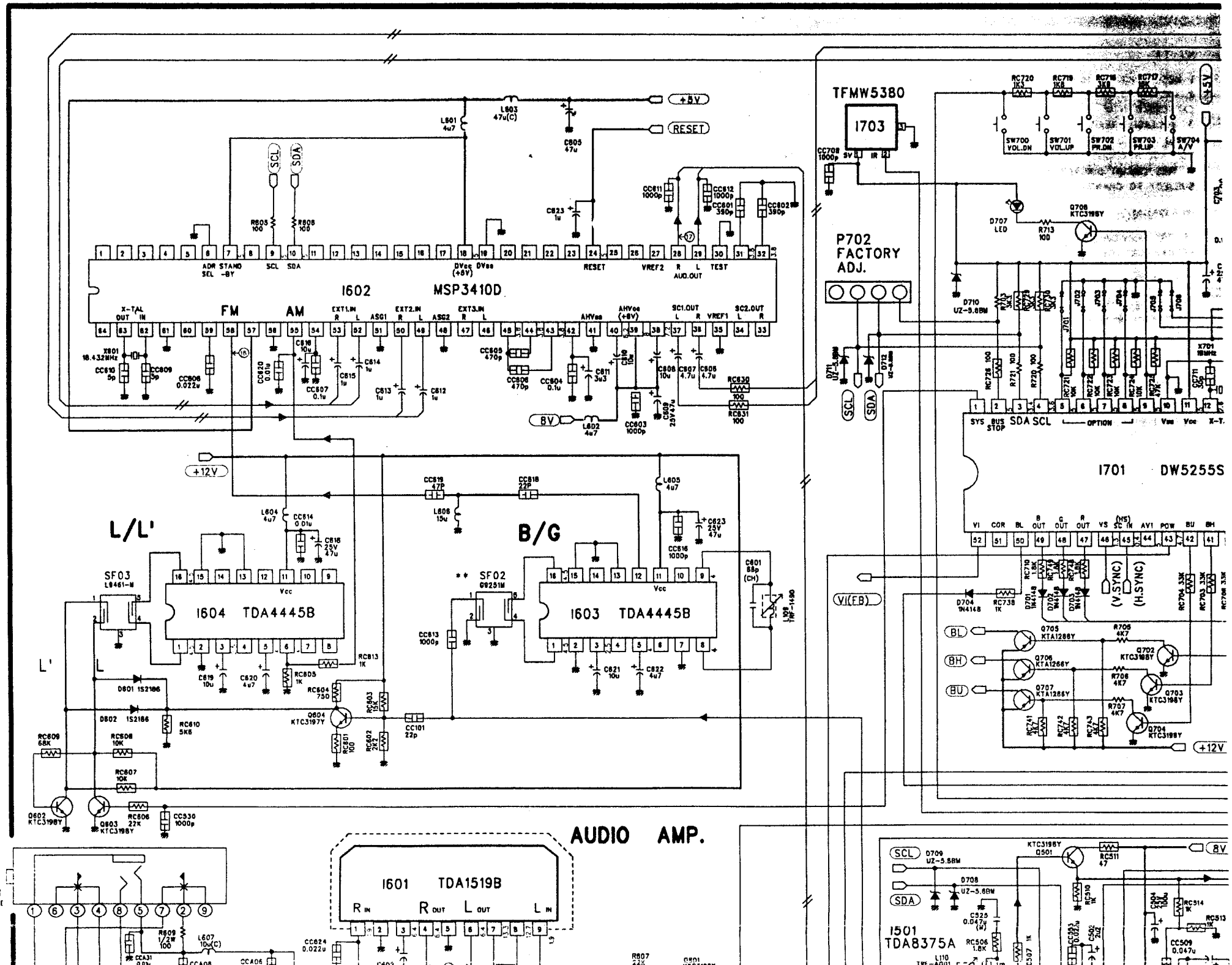
THE DIFFERENT PARTS FOR CRT (CP-775)

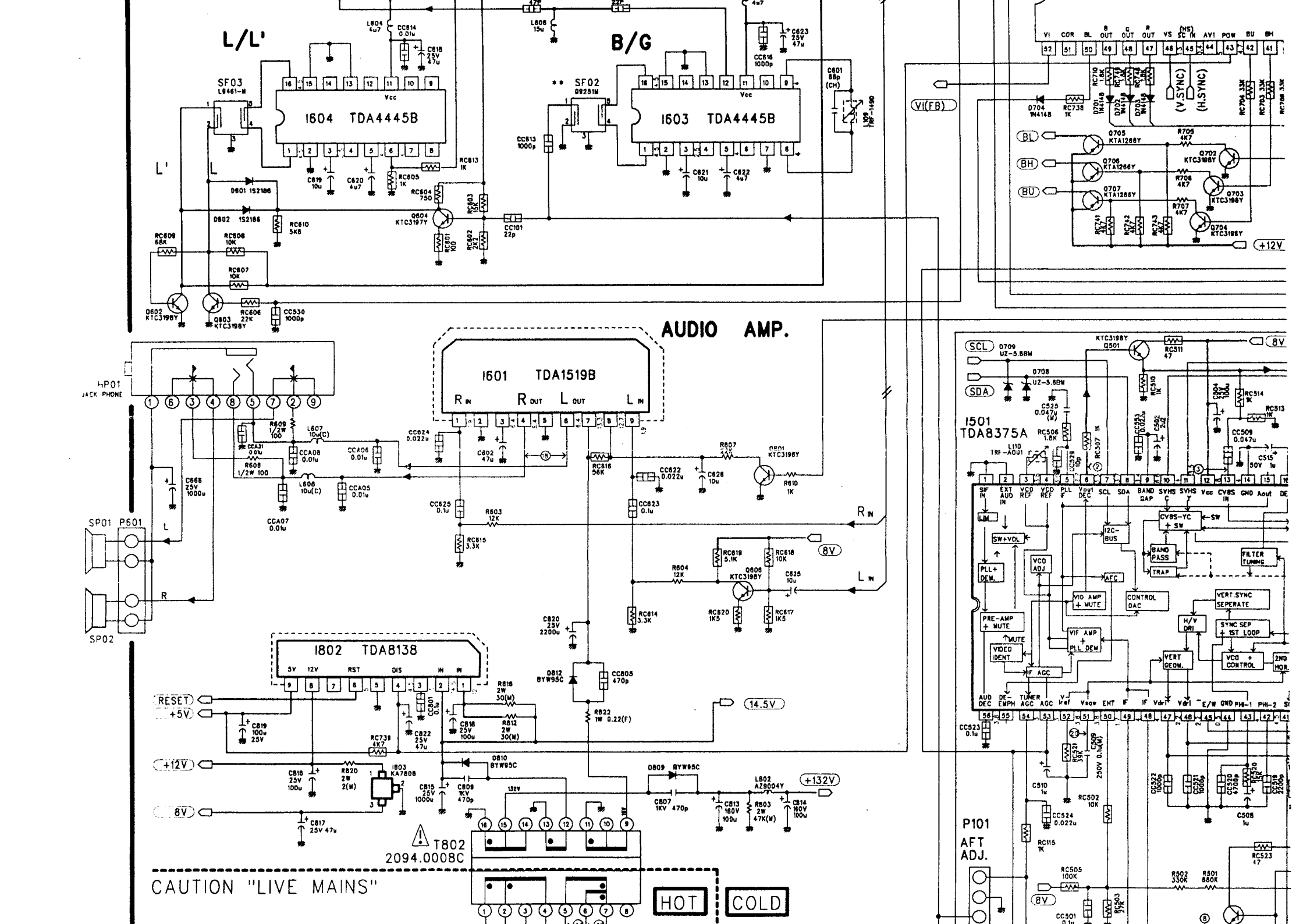
No	LOC.	NAME	28" (V/COLOR)	28"(PHILIPS)	25"(PHILIPS)	29"(ORION)
1	C402	C MYLAR	1.6KV 7200PF	←	←	←
			CMYH3C722J			
2	C404	C MYLAR	1.6KV 4700PF	←	←	1.6KV 8200PF
			CMYH3C472J			CMYH3C822J
3	C408	C MYLAR	400V 0.27MF	←	←	400V 0.51MF
			CMYE2G274J			CMYE2G514J
4	D406	DIODE	BYW95X	←	←	×
			DBYW95C - - -			
5	J802	WIRE COPPER	×	×	×	AWG22 1/0.65 TIN
						COATING
						85801065GY
6	R333	R C-FILM	1/4W 2K OHM	1/4W 3K OHM	←	1/4W 2K OHM
			RD-4Z202J -	RD-4Z302J-		RD-4Z202J -
7	R919	R FUSIBLE	1W 0.68	1W 3.3	←	1W 0.68
			RF01Z688J -	RF01Z339J -		RF01Z688J -
8	V901	CRT	A66ECY13X611	A66EAK071X11	A59EAK071X11	A68KTB140X010
			4859613360	4859622160	4859622260	485961976 *
9	ZDC10	COIL	DC-2701	←	DC-2501	
		DEGAUSSING	58G0000103		58G719M096	

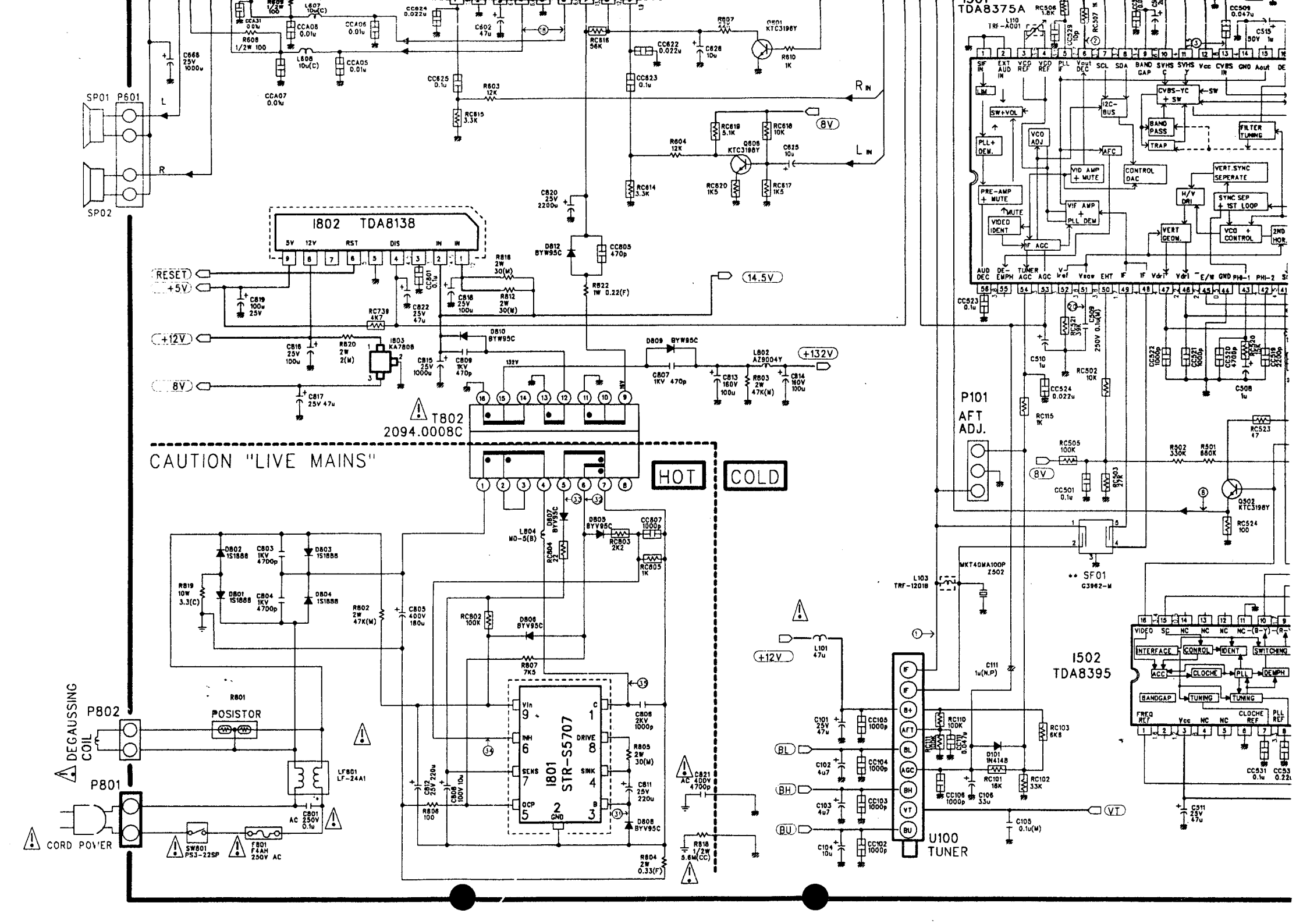
THE DIFFERENT PARTS FOR SYSTEM (CP-775)

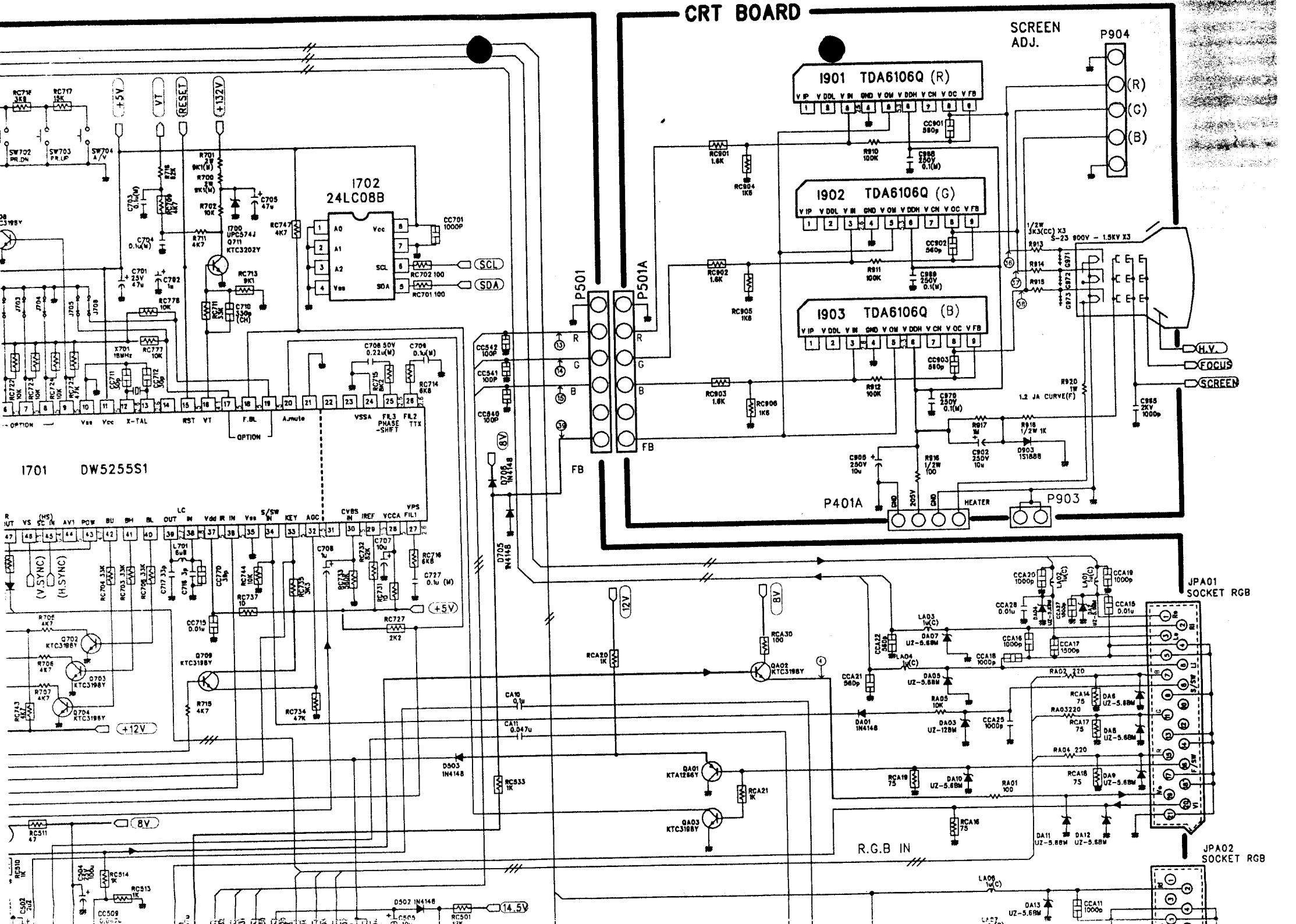
No	LOC.	NAME	TF	TU	TK	TA
1	J701	WIRE COPPER	×	×	AWG22 1/0.65 TIN COATING 85801065GY	×
2	J702	WIRE COPPER	×	×	×	×
3	J703	WIRE COPPER	×	×	AWG22 1/0.65 TIN COATING 85801065GY	×
4	J704	WIRE COPPER	×	AWG22 1/0.65 TIN COATING 85801065GY	×	×
5	J705	WIRE DOPPER	×	×	×	AWG22 1/0.65 TIN COATING 85801065GY
6	J706	WIRE COPPER	×	×	×	×
7	SF01	FILTER SAW	G3962M 5PG3962M - -	G3962M 5PG3962M - -	G3962M 5PG3962M - -	G3962M 5PG3962M - -
8	SF02	FILTER SAW	G9251M 5PG9251M - -	K9260M 5PK9260M - -	K9260M 5PK9260M - -	G9251M 5PG9251M - -
9	SF03	FILTER SAW	×	×	×	L9461M 5PL9461M - -
10	Z502	FILTER CERA	MKT40MA100P 5PMKT40MA -	MKT40MA100P 5PMKT40MA -	×	MKT40MA100P 5PMKT40MA -
11	I502	IC	×	×	TDA8395 1TDA8395 - -	TDA8395 1TDA8395 - -
12	I604	IC	×	×	×	TDA4445B TDA4445B -
13	U100	TUNER VATACTOR	3303KHC 4859714430	DT2-IV17D 4859716130	3303KHC 4859714430	3303KHC 4859714430
14	P801	CORD POWER AS	CW4232+BL102NG +TUBE=2500 4859903110	CW3222/240V 5A +HOUS=2200 4859905110	KKP419C+BL102NG +TUBE+2100 4859902910	CW4232+BL102NG +TUBE=2500 4859903110
15	D601	DIODE	×	×	×	1S2186 D1S2186 - - -
16	D602	DIODE	×	×	×	1S2186 D1S2186 - - -

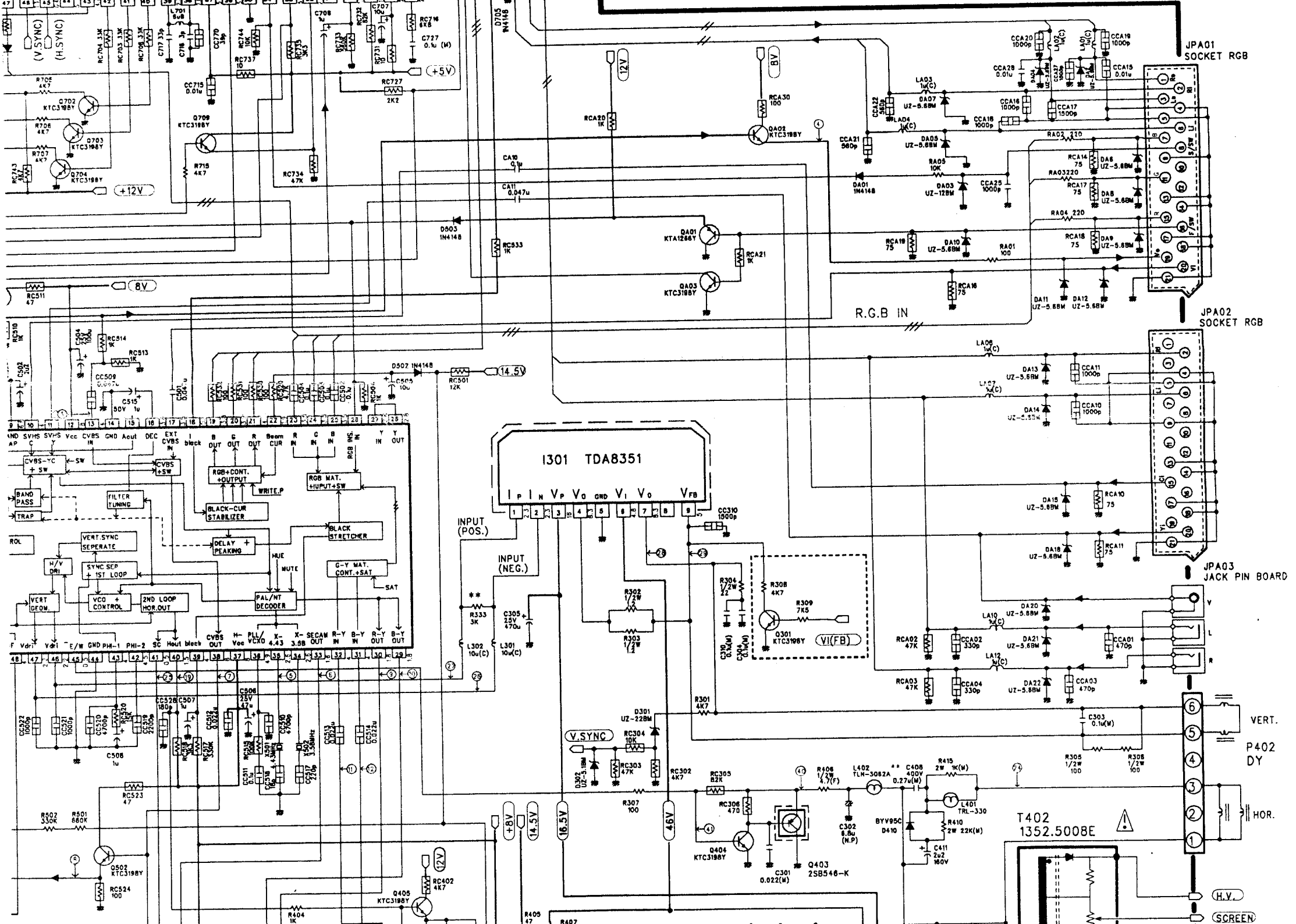

CP-775 MAIN
S/N:4859801393-01
CAUTION "LIVE MAINS"
F4AH 250V AC
AC INPUT
T802
T402
I801
I701
I702
I601
I301
I501
I502
I503
I602
I603
I604
I802
RGB
SCT1
STC2
TV/AV
VOL DN
VOL UP
CH DN
CH UP
BOOST
AFC HEATER ABL
U100

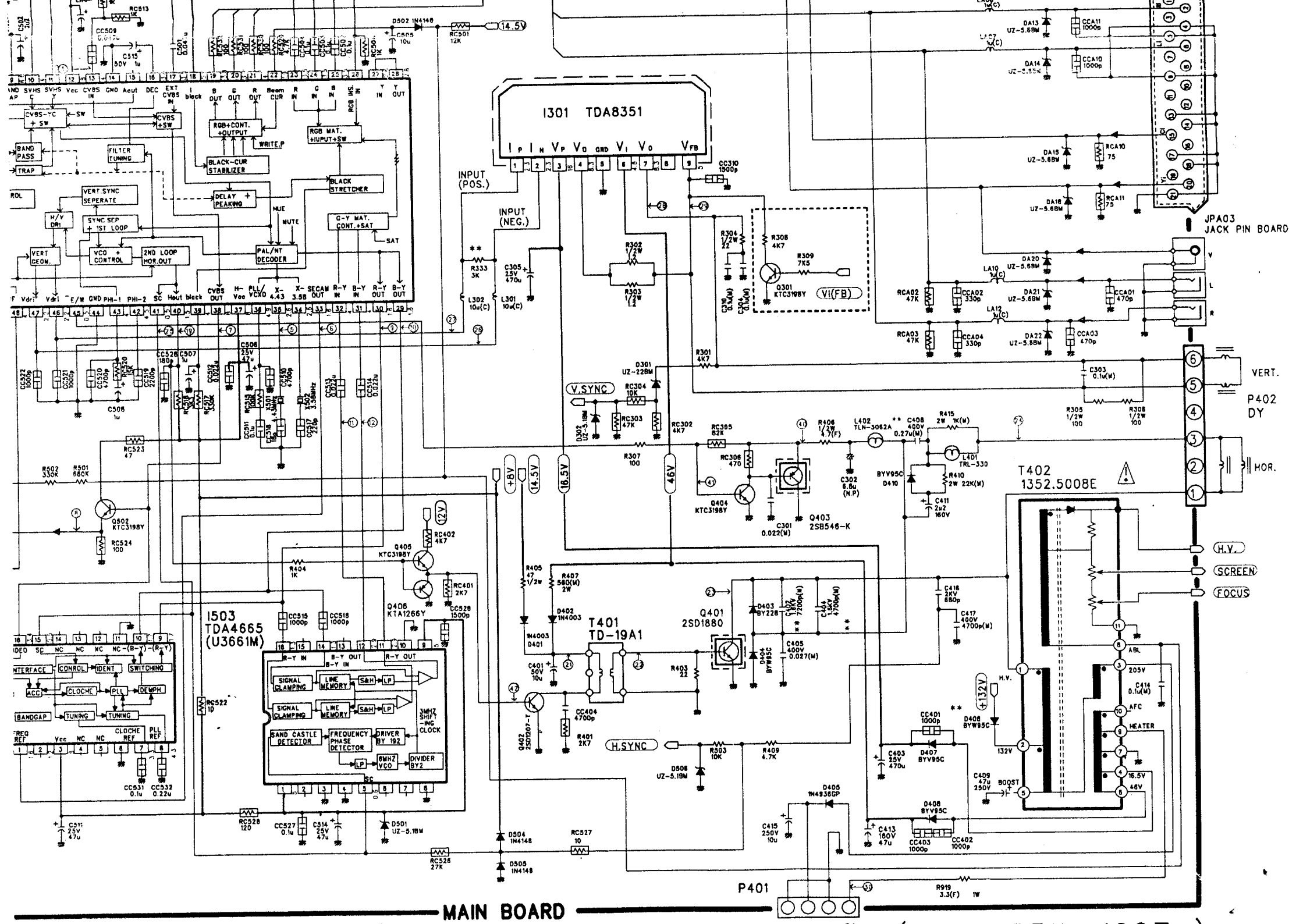

TFMW5380
1703
P702
FACTORY
ADJ.
1602 MSP3410D
1701 DW5255S
1604 TDA4445B
1603 TDA4445B
L/L'
B/G
AUDIO AMP.
1601 TDA1519B
1501
TDA8375A
SF03
SF02
+5V
+12V
8V
RESET
SCL
SDA
VI(FB)
(V SYNC)
(H.SYNC)
BL
BH
BU
HP01
JACK PHONE


L/L'
B/G
AUDIO AMP.
SF03
L9461-M
1604 TDA4445B
** SF02
G9251M
1603 TDA4445B
1601 TDA1519B
R IN
R OUT
L OUT
L IN
1501
TDA8375A
1802 TDA8138
5V
12V
RST
DIS
IN
IN
HP01
JACK PHONE
SP01
P601
SP02
L
R
RESET
+5V
+12V
8V
14.5V
+132V
T802
2094.0008C
CAUTION "LIVE MAINS"
HOT
COLD
P101
AFT
ADJ.
SCL
SDA
VI(FB)
BL
BH
BU
+12V
V.SYNC
H.SYNC
KTC3198Y
Q501
D709
UZ-5.6BM
D708
UZ-5.6BM
VCO ADJ
AFC
I2C-BUS
CVBS-YC + SW
BAND PASS
TRAP
FILTER TUNING
PLL+ DEM.
SW+VOL
PRE-AMP + MUTE
VID AMP + MUTE
CONTROL DAC
VIF AMP + PLL DEM
VERT.SYNC SEPERATE
H/V DRI
SYNC SEP + 1ST LOOP
VERT GEOM.
VCO + CONTROL
HF AGC
VIDEO IDENT
MUTE
L601
10u(C)
L606
10u(C)
L607
10u(C)
L602
15u
L604
4u7
L608
15u
D601 1S2186
D602 1S2186
Q604 KTC3197Y
Q605 KTA1268Y
Q606 KTA1268Y
Q607 KTA1268Y
Q702 KTC3198Y
Q703 KTC3198Y
Q704 KTC3198Y
Q602 KTC3198Y
Q603 KTC3198Y
Q801 KTC3198Y
Q606 KTC3198Y
D810 BYW95C
D809 BYW95C
D812 BYW95C
I803 KA7808
L802 AZ9004Y


SP01
P601
SP02
L
R
C666 25V 1000u
CCA31 0.0u
CCA08 0.01u
CCA06 0.01u
CCA07 0.01u
CCA05 0.01u
R608 1/2W 100
L608 10u(C)
L607 10u(C)
CC824 0.022u
C602 47u
RC816 56K
CC625 0.1u
R603 12K
RC615 3.3K
CC622 0.022u
C626 10u
Q601 KTC3198Y
R610 1K
CC623 0.1u
R607 2K2
R IN
L IN
8V
RC619 5.1K
RC618 10K
R604 12K
Q606 KTC3198Y
C625 10u
RC614 3.3K
RC620 1K5
RC617 1K5
C820 25V 2200u
D812 BYW95C
CC805 470p
R822 1W 0.22(F)
14.5V
I802 TDA8138
5V 12V RST DIS IN IN
RESET
+5V
C819 100u 25V
CC801 0.1u
C818 25V 100u
R818 2W 30(M)
R812 2W 30(M)
C822 25V 47u
RC739 4K7
+12V
C816 25V 100u
R820 2W 2(M)
I803 KA7808
C815 25V 1000u
C809 1KV 470p
D810 BYW95C
132V
D809 BYW95C
L602 AZ9004Y
+132V
C807 1KV 470p
C813 160V 100u
R603 2W 47K(M)
C814 160V 100u
8V
C817 25V 47u
T802
2094.0008C
CAUTION "LIVE MAINS"
HOT
COLD
D802 1S1888
C803 1KV 470p
D803 1S1888
D801 1S1888
C804 1KV 470p
D804 1S1888
R819 10W 3.3(C)
R802 2W 47K(M)
C805 400V 180u
L804 MD-5(B)
D807 BYV95C
D805 BYV95C
CC807 1000p
RC804 22
RC803 2K2
RC805 1K
RC802 100K
D806 BYV95C
R807 7K5
R801
POSISTOR
P802
DEGAUSSING COIL
P801
LF801 LF-24A1
AC
C801 250V 0.1u
CORD POWER
SW801 PS3-22SP
F801 F4AH 250V AC
I801 STR-S5707
Vin
INH
SENS
OCP
C
DRIVE
SINK
B
GND
CB12 25V 220u
CB06 100V 10u
R806 100
CB08 2KV 1000p
R805 2W 30(M)
C811 25V 220u
D808 BYV95C
C821 400V 4700p
R818 1/2W 5.6M(CC)
R804 2W 0.33(F)
TDA8375A
L110 TRF-A001
RC506 1.8K
RC307 1K
CC523 10p
CC509 0.047u
C515 50V 1u
SIF IN
EXT AUD IN
VCO REF
VCO REF
PLL IF
Vout DEC
SCL
SDA
BAND GAP
SVHS Y
SVHS C
Vcc
CVBS IN
GND
Aout
DE
LIM
SW+VOL
PLL+ DEM.
VCO ADJ
I2C-BUS
CVBS-YC + SW
BAND PASS
TRAP
FILTER TUNING
AFC
VID AMP + MUTE
CONTROL DAC
VERT.SYNC SEPERATE
PRE-AMP + MUTE
MUTE
VIDEO IDENT
VIF AMP + PLL DEM
H/V DRI
SYNC SEP + 1ST LOOP
IF AGC
VERT GEOM.
VCO + CONTROL
2ND HOR.
AUD DEC
DE-EMPH
TUNER AGC
AGC
Vref
Vsaw
EMT
IF
IF
Vdri
Vdri
E/W
GND
PHI-1
PHI-2
CC523 0.1u
RC521 39K
C509 0.1u(M)
250V
C510 1u
RC502 10K
CC524 0.022u
RC115 1K
P101
AFT
ADJ.
RC505 100K
R502 330K
R501 680K
R503 33K
CC501 0.1u
Q502 KTC3198Y
RC524 100
RC523 47
C508 1u
** SF01
G3962-M
L103 TRF-12018
MKT40MA100P Z502
+12V
L101 47u
C111 1u(N.P)
C101 25V 47u
CC105 1000p
C102 4u7
CC104 1000p
C103 4u7
CC103 1000p
C104 10u
CC102 1000p
BL
BH
BU
VT
IF
IF
B+
AFT
BL
AGC
BH
VT
BU
RC110 100K
RC111 150K
CC111 0.047u
D101 1N4148
RC101 18K
RC103 6K8
RC102 33K
CC106 1000p
C106 33u
C105 0.1u(M)
U100 TUNER
I502 TDA8395
VIDEO
SC
NC
NC
NC
NC
-(B-Y)-
-(R-
INTERFACE
CONTROL
IDENT
SWITCHING
ACC
CLOCHE
PLL
DEMPH
BANDGAP
TUNING
TUNING
FREQ REF
Vcc
NC
NC
CLOCHE REF
PLL REF
CC531 0.1u
CC53 0.22u
C511 25V 47u


CRT BOARD
SCREEN ADJ.
P904
(R)
(G)
(B)
I901 TDA6106Q (R)
I902 TDA6106Q (G)
I903 TDA6106Q (B)
P501
P501A
R
G
B
FB
H.V.
FOCUS
SCREEN
P401A
P903
HEATER
I702
24LC08B
SCL
SDA
I701 DW5255S1
+5V
VT
RESET
+132V
+12V
8V
14.5V
(V.SYNC)
(H.SYNC)
JPA01
SOCKET RGB
JPA02
SOCKET RGB
R.G.B IN


I301 TDA8351
I P I N V P V O GND V I V O V FB
R.G.B IN
JPA01 SOCKET RGB
JPA02 SOCKET RGB
JPA03 JACK PIN BOARD
T402 1352.5008E
P402 DY
VERT.
HOR.
H.V.
SCREEN
INPUT (POS.)
INPUT (NEG.)
V.SYNC
(V.SYNC)
(H.SYNC)
+5V
+12V
8V
14.5V
16.5V
46V
VI(FB)
CVBS-YC + SW
CVBS +SW
RGB+CONT. +OUTPUT
RGB MAT. +INPUT+SW
BLACK-CUR STABILIZER
BLACK STRETCHER
DELAY + PEAKING
FILTER TUNING
VERT.SYNC SEPERATE
SYNC SEP + 1ST LOOP
VCO + CONTROL
2ND LOOP HOR.OUT
PAL/NT DECODER
G-Y MAT. CONT.+SAT
WRITE.P
BAND PASS
TRAP
H/V DRI
VERT GEOM.
MUTE
HUE
SAT
Q301 KTC3198Y
Q302 KTC3198Y
Q303 KTC3198Y
Q304 KTC3198Y
Q401 KTA1266Y
Q402 KTC3198Y
Q403 2SB546-K
Q404 KTC3198Y
Q405 KTC3198Y
Q502 KTC3198Y
Q503 KTC3198Y
Q709 KTC3198Y
D301 UZ-228M
D302 UZ-5.1BM
D401 BYV95C
L401 TRL-330
L402 TLN-3062A
L301 10u(C)
L302 10u(C)
T501 4.43MHz
T502 3.58MHz


I301 TDA8351
I P I N V P V O GND V I V O V FB
INPUT (POS.)
INPUT (NEG.)
VERT.SYNC SEPERATE
SYNC.SEP + IST LOOP
VCO + CONTROL
2ND LOOP HOR.OUT
PAL/NT DECODER
BLACK-CUR STABILIZER
DELAY PEAKING
BLACK STRETCHER
RGB+CONT. +OUTPUT
RGB MAT. +INPUT+SW
G-Y MAT. CONT.+SAT
FILTER TUNING
BAND PASS
TRAP
CVBS-Y/C + SW
CVBS +SW
WRITE.P
HUE
MUTE
SAT
V.SYNC
H.SYNC
I503 TDA4665 (U3661M)
SIGNAL CLAMPING
LINE MEMORY
S&H
LP
SAND CASTLE DETECTOR
FREQUENCY PHASE DETECTOR
DRIVER BY 192
6MHZ VCO
DIVIDER BY2
3MHZ SHIFT -ING CLOCK
T401 TD-19A1
Q401 2SD1880
Q402 2SD1207-T
Q403 2SB546-K
Q404 KTC3198Y
Q405 KTC3198Y
Q406 KTA1266Y
Q502 KTC3198Y
T402 1352.5008E
L401 TRL-530
L402 TLN-3062A
P401
P402 DY
JPA03 JACK PIN BOARD
VERT.
HOR.
H.V.
SCREEN
FOCUS
ABL
205V
AFC
HEATER
16.5V
46V
132V
BOOST
+8V
14.5V
16.5V
46V
12V
+132V

MAIN BOARD

CHASSIS : CP - 775

SCHEMATIC DIAGRAM

* PAL - B/G
* PAL/SECAM - B/G, D/K
  NTSC - 3.58/4.43 (AV)
* PAL/SECAM - B/G, D/K
  SECAM - L
* PAL - I

RESISTOR

CARBON FILM	
R M-OXIDE	(M)
CARBON COMP	(CC)
FUSIBLE	(F)
CEMENT	(C)
CHIP	

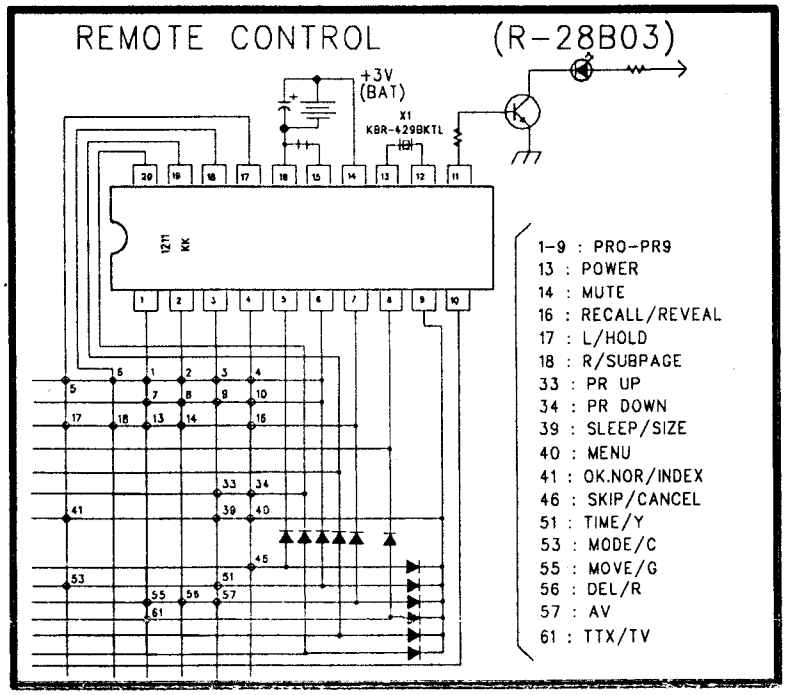
CAPACITOR

ELECTRO	
CERAMIC	
CERAMIC CH	(CH)
ELECTRO NONPOLAR	(NP)
MYLAR	(M)
CHIP	

COIL

PEAKING	
CHOKE	(C)
BEAD	(B)

REMOTE CONTROL (R-28B03)



THE DIFFERENT PARTS FOR CRT

LOC.	25 INCH PHILIPS	28 INCH PHILIPS	28 INCH V/COLOR	29 INCH ORION
C402	1.5KV 7200pF(M)	←	←	←
C404	1.6KV 4700pF(M)	←	←	1.6KV 8200pF(M)
C408	400V 0.27uF(M)	←	←	400V 0.51uF(M)
D406	BYW95C	←	←	x
J802	x	x	x	JUMPER
R333	1/4W 3K OHM	←	1/4W 2K OHM	1/4W 2K OHM

NOTE:

1. RESISTANCE IS SHOWN IN OHM. K=1000, M=1000000
2. UNLESS OTHERWISE NOTED IN SCHEMATIC ALL CAPACITOR VALUES ARE EXPRESSED IN uF .
3. VOLTAGES READ WITH "VTVM" FROM POINT INDICATED TO CHASSIS GROUND USING A COLOR BAR SIGNAL WITH ALL CONTROLS AT NORMAL LINE 230V AC VOLTAGE READINGS SHOWN ARE NORMAL VALUES AND MAY VARY ±20% EXCEPT H.V
4. THIS CIRCUIT DIAGRAM IS A STANDARD ONE CIRCUIT PRINTED MAY BE SUBJECT TO CHANGE FOR PRODUCT IMPROVEMENT WITHOUT PRIOR NOTICE .

WARNING:

BEFORE SERVICING THE CHASSIS, READ "X-RAY RADIATION", "SAFETY PRECAUTION", AND "PRODUCT SAFETY NOTICE" IN SERVICE MANUAL .

CAUTION TO SERVICE TECHNICIANS:

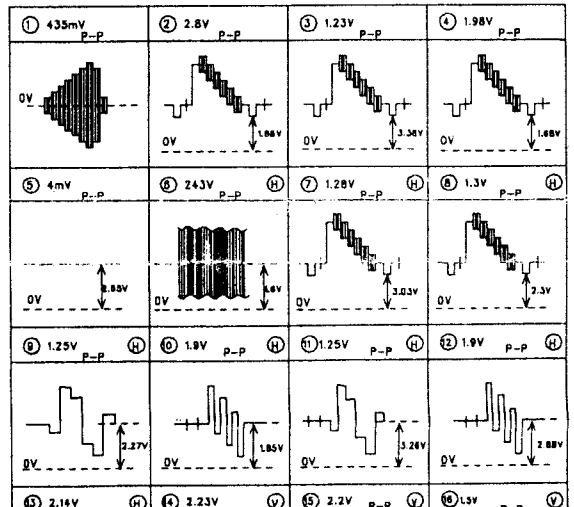
BEFORE RETURNING THE RECEIVER TO CUSTOMER, LEAKAGE CURRENT OR RESISTANCE MEASUREMENTS SHOULD BE PERFORMED TO DETERMINE THAT EXPOSED PARTS ARE PROPERLY INSULATED FROM THE SUPPLY CIRCUIT.

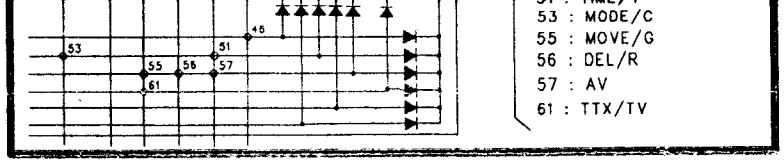
PRODUCT SAFETY NOTE :

THE COMPONENTS MARKED WITH ⚠ ARE IMPORTANT FOR MAINTAINING THE SAFETY OF THE SET AND SHOULD BE REPLACED ONLY WITH TYPES IDENTICAL TO THOSE IN THE ORIGINAL OR SPECIFIED ONE IN THE PART LIST. DON'T DEGRADE THE SAFETY OF THE SET THROUGH IMPROPER SERVICING.

WAVE FORMS

INPUT SIGNAL : PAL SYSTEM
VIDEO : 8 STEP COLOR BAR 87.5% AM
CONTROL ALL MAX MODE
AUDIO : 1KHz SINE WAVE 60% FM





THE DIFFERENT PARTS FOR CRT

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C404	1.6KV 4700pF(M)	←	←	1.6KV 8200pF(M)
C408	400V 0.27uF(M)	←	←	400V 0.51uF(M)
D406	BYW95C	←	←	x
JB02	x	x	x	JUMPER
R333	1/4W 3K OHM	←	1/4W 2K OHM	1/4W 2K OHM
R919	1W 3.3 (F)	←	1W 0.68 (F)	1W 0.68 (F)

OPTION

#5	#6	#7	#8	#17	#19	TTX	TUNING/SOUND SYSTEM	ATS
H	H					WEST TTX		
L	H					EAST TTX		
H	L					TURKEY TTX		
		L	H	H			B/G (2-C, NICAM)	
		H	H	H			B/G, D/K (2-C, NICAM)	
		L	L	H			I/I (NICAM)	
		H	L	H			I (UHF ONLY , NICAM)	
		H	H	L			L/L' B/G (2-C, NICAM)	
		L	H	L			B/G, L/L' (2-C, NICAM)	
					H			ATS ON
					L			ATS OFF

THE DIFFERENT PARTS OF SYSTEM

SYSTEM		PAL-B/G	PAL-I	P/S-B/G, D/K	P/S-B/G, SECAM-L/L'
1	J701	X	X	JUMPER	X
2	J702	X	X	X	X
3	J703	JUMPER	X	X	X
4	J704	X	JUMPER	X	X
5	J705	X	X	X	JUMPER
6	J706	X	X	X	X
7	SF01	G3962M	G3962M	G3962M	G3962M
8	SF02	G9251M	K9260M	K9260M	G9251M
9	SF03	X	X	X	L9461M
10	Z502	MKT40MA	MKT40MA	X	MKT40MA
11	I502	X	X	TDA8395	TDA8395
12	I604	X	X	X	TDA4445B
13	U100	3303KHC	DT2-IV17D	3303KHC	3303KHC
14	P801	CW-4232	CW-3222	KKP-419C	CW-4232
15	D601	X	X	X	1S2186
16	D602	X	X	X	1S2186